EXHIBIT A

DOCKET NO.: 1745950-00120US3
Filed on behalf of STMicroelectronics, Inc.
By: Scott Bertulli, Reg. No. 75,886 (Lead Counsel)
Richard Goldenberg, Reg. No. 38,895 (Backup Counsel)
Gregory Lantier (*pro hac vice* to be filed) (Backup Counsel)
Trishan Esram, Reg. No. 74,075 (Backup Counsel)
Wilmer Cutler Pickering Hale and Dorr LLP
60 State Street
Boston, MA 02109
Email: scott.bertulli@wilmerhale.com
richard.goldenberg@wilmerhale.com
gregory.lantier@wilmerhale.com
trishan.esram@wilmerhale.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.
Petitioner

v.

THE TRUSTEES OF PURDUE UNIVERSITY
Patent Owner

IPR2022-00723
U.S. Patent No. 7,498,633

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,498,633 CHALLENGING CLAIMS 1–8 AND 12–15 UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

TABLE OF CONTENTS

Page

STMicroelectronics, Inc. ("Petitioner") respectfully requests *inter partes* review ("IPR") of claims 1–8 and 12–15 of U.S. Patent No. 7,498,633 (the "'633 patent") (EX1001).

I. INTRODUCTION

The '633 patent is directed to semiconductor devices, such as metal-oxide semiconductor field-effect transistors (MOSFETs), for high-voltage power applications. The problem described by the '633 patent and its alleged solution, however, were well-known in the art.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner STMicroelectronics, Inc. ("ST") is a real party-in-interest. Although STMicroelectronics N.V., ST's parent company, and STMicroelectronics International N.V., which is under common ownership with ST, are not real parties-in-interest under the governing legal standard for making that determination, ST identifies them as real parties-in-interest for purposes of this Petition to avoid any disputes over that issue.

B. Related Matters

According to USPTO records, the '633 patent is owned by The Trustees of Purdue University ("Patent Owner" or "PO"). Petitioner knows of the following co-pending litigations involving the '633 patent: *The Trustees of Purdue University v.*

STMicroelectronics N.V. and STMicroelectronics, Inc., No. 6:21-CV-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.). Petitioner is challenging claims 9–11 of the '633 patent in co-pending IPR2022-00252. Petitioner is also aware that Wolfspeed, Inc. filed a petition challenging claims 9–11 of the '633 patent on March 25, 2022 in IPR2022-00761. The earliest date of service on Petitioner in the co-pending litigation was July 20, 2021.

C. Counsel

Under 37 C.F.R. §§ 42.8(b)(3)–(4), Petitioner identifies the following lead and backup counsel, to whom all correspondence should be directed.

Lead Counsel:	Scott Bertulli (Reg. No. 75,886)
Backup Counsel:	Richard Goldenberg (Reg. No. 38,895)
	Gregory Lantier (*pro hac vice* to be filed)
	Trishan Esram (Reg. No. 74,075)

D. Service Information

E-mail:	scott.bertulli@wilmerhale.com
	richard.goldenberg@wilmerhale.com
	gregory.lantier@wilmerhale.com
	trishan.esram@wilmerhale.com
Post and hand delivery:	Wilmer Cutler Pickering Hale and Dorr LLP

60 State Street

Boston, MA 02109

Telephone: 617-526-6223

Fax: 617-526-5000

Petitioner consents to service by e-mail on lead and backup counsel.

III. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") at the time of the earliest claimed priority date[1] of the '633 patent would have had the equivalent of a Bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices. Less work experience may be compensated by a higher level of education, such as a Master's Degree, and vice versa. EX1035, ¶23.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that the patent for which review is sought is available for IPR and under 37 C.F.R. §§ 42.101(a)–(c) that

[1] The '633 patent claims priority to U.S. Provisional Application No. 60/646,152 filed on January 21, 2005. Petitioner does not concede—and does not believe—that any of the challenged claims are entitled to benefit of that provisional application. Regardless, the references relied upon herein are prior art.

Petitioner is not barred or estopped from requesting an IPR challenging the patent claims on the ground identified in this Petition.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Claims for Which Review is Requested and Ground on Which the Challenge is Based

Under 37 C.F.R. §§ 42.22(a)(1) and 42.104(b)(1)–(2), Petitioner requests cancellation of claims 1–8 and 12–15 of the '633 patent on the following ground:

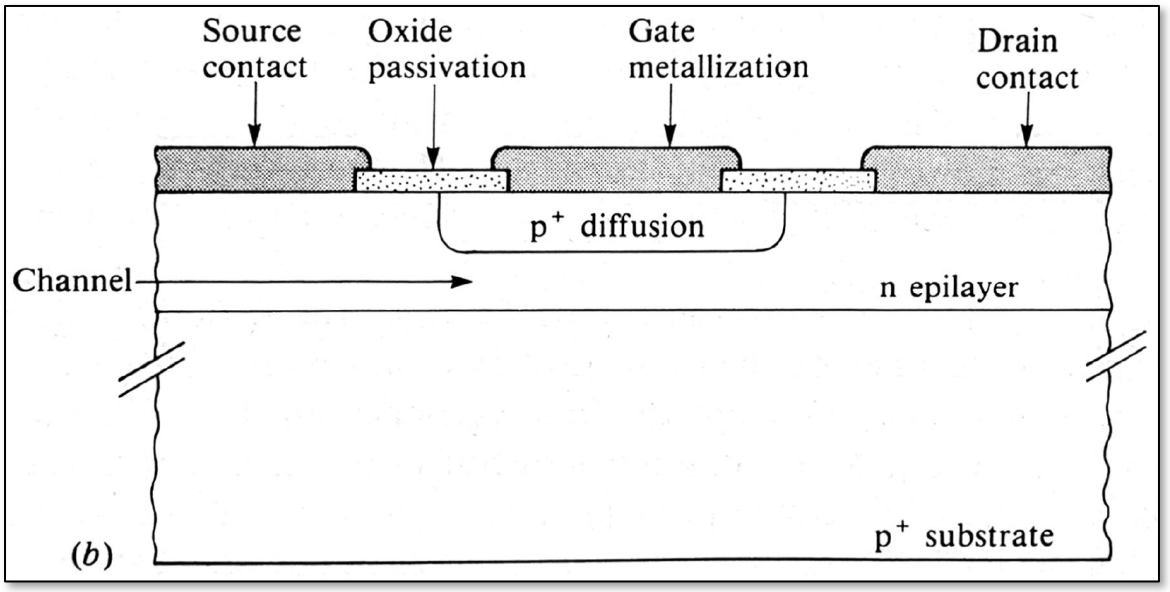
Ground	References	Basis	Claims Challenged
I	*Ryu* in view of *Williams*	§ 103	1–8 and 12–15

This Petition, supported by the declaration of Dr. Subramanian (EX1035), demonstrates that there is a reasonable likelihood Petitioner will prevail with respect to cancellation of at least one of the challenged claims. *See* 35 U.S.C. § 314(a).

VI. TECHNOLOGY BACKGROUND

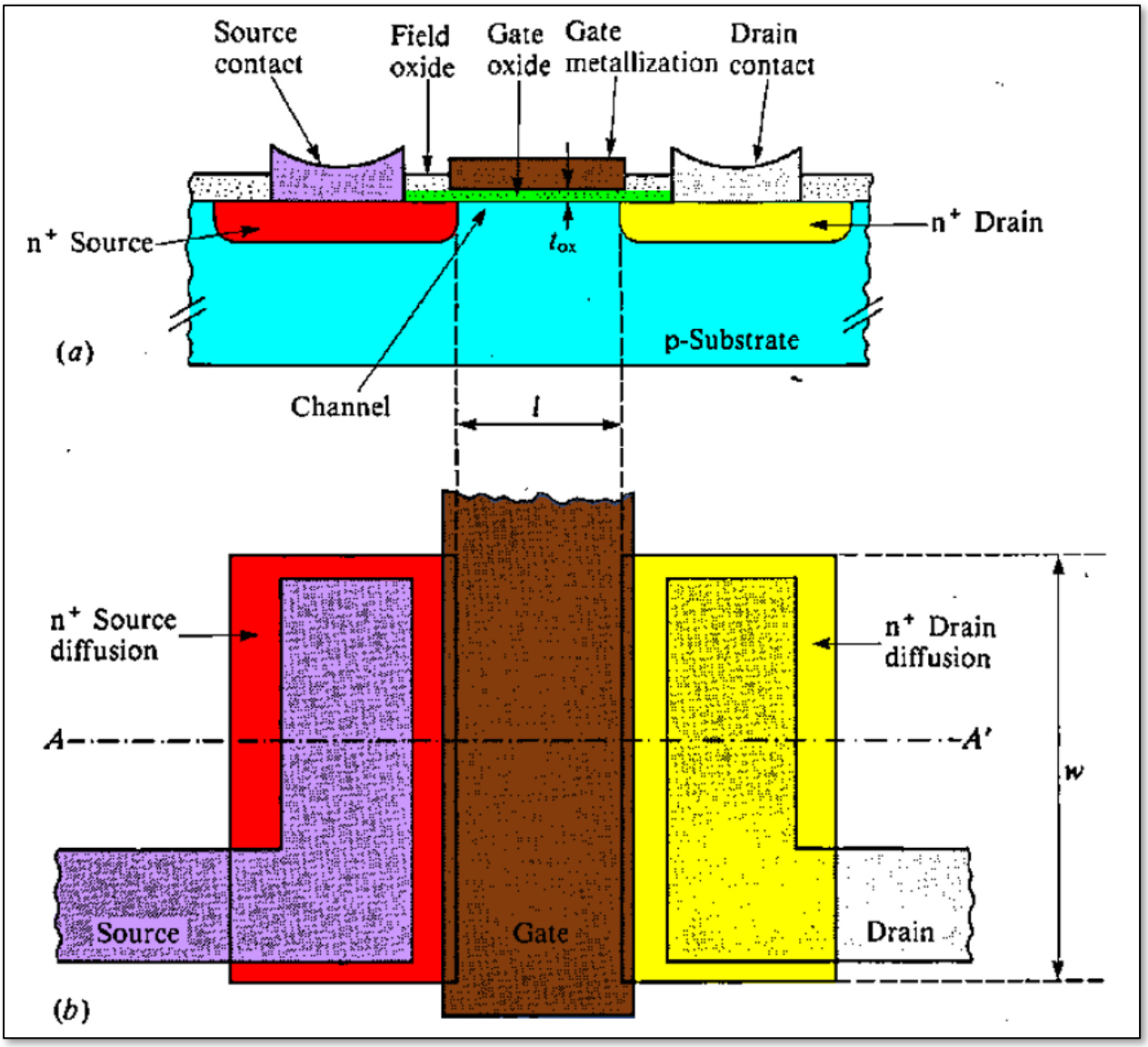
A. Field-Effect Transistor

A field-effect transistor ("FET") is a type of transistor that uses an electric field to control the flow of current in a semiconductor. *See* "Power MOSFETs – Theory and Applications," Duncan A. Grant et al. ("*Grant*"), EX1019, 1. A FET generally includes a source, a drain, and a gate, as *Grant* illustrates in a cross section of a junction field-effect transistor (JFET) in Figure 1.1, below. *See, e.g.*, *id.*, 2. EX1035, ¶¶24–26.



EX1019, Figure 1.1

"[T]echnological refinements in the early 1960s enabled . . . the metal-oxide-semiconductor field-effect transistor (MOSFET)." EX1019, 5. The difference between a JFET and a MOSFET is "[t]he controlling gate electrode is now separated from the semiconductor by a thin insulating layer of gate oxide, as shown in Figure 1.3." *Id.*; *see also* U.S. Patent No. 5,233,215 ("*Baliga*") (EX1005), 1:45–50. Figure 1.3 (below), shows a MOSFET with the source region annotated in red, drain region in yellow, p-type substrate in cyan, gate in brown, gate oxide in green, and source contact in lavender. The source contact is often referred to as "source metallization," "source metal," or "source electrode." *See* EX1019, Figure 1.13; EX1015, Figure 1, 1:38; EX1005, 2:64. EX1035, ¶27.

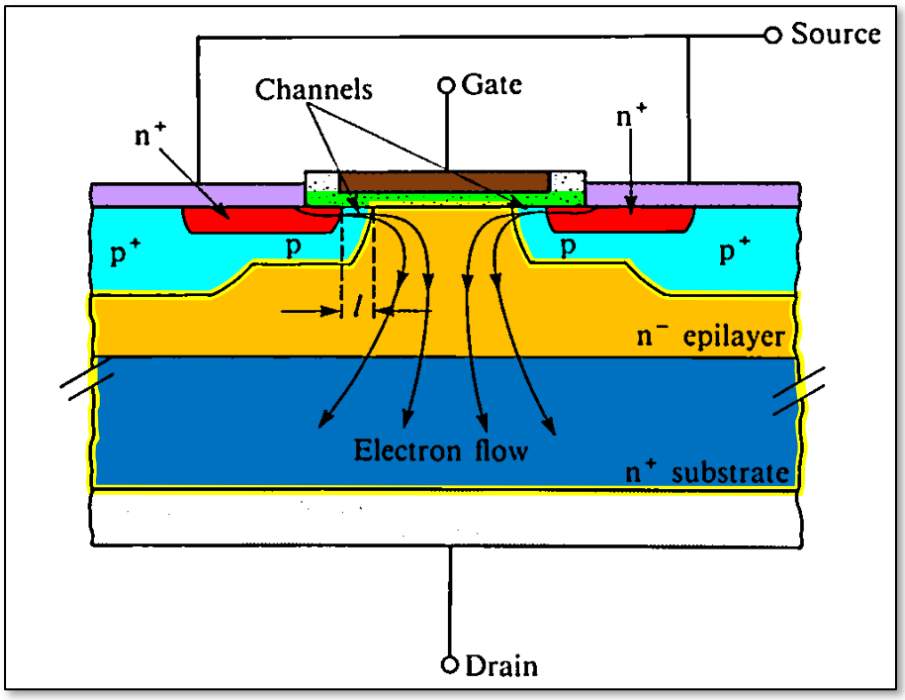


EX1019, Figure 1.3 (annotated)

B. Power MOSFET

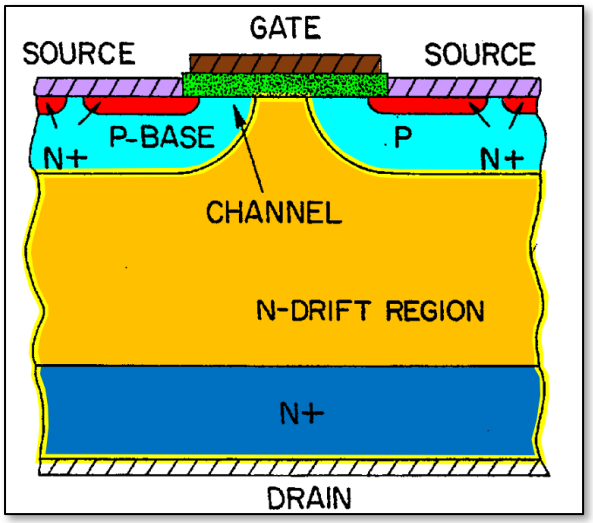
The MOSFET became "important in devices designed for power applications." EX1019, 5; *see also* EX1005, 2:14–16. *Grant* notes that "the decision as to what constitutes a power device is quite arbitrary" and the term is applied to "any device capable of switching at least 1 A." EX1019, 5–6. EX1035, ¶28.

Grant found "the planar structure of Figure 1.3 [] unsatisfactory if it is simply scaled up for higher powers." EX1019, 8. One well-known solution was to change the planar structure to a vertical structure that uses the substrate material to form the drain region such that "the current flows 'vertically' through the silicon from drain to source." *Id.* This change led to the ***vertical double-diffused MOSFET***, which *Grant* illustrates in Figure 1.11 (below). *Id.*, 13–14. EX1035, ¶29.



EX1019, Figure 1.11 (annotated)

Baliga also illustrates a vertical double-diffused MOSFET in Figure 1 (below). EX1005, 6:12–13. EX1035, ¶30.



EX1005, FIG. 1 (annotated)

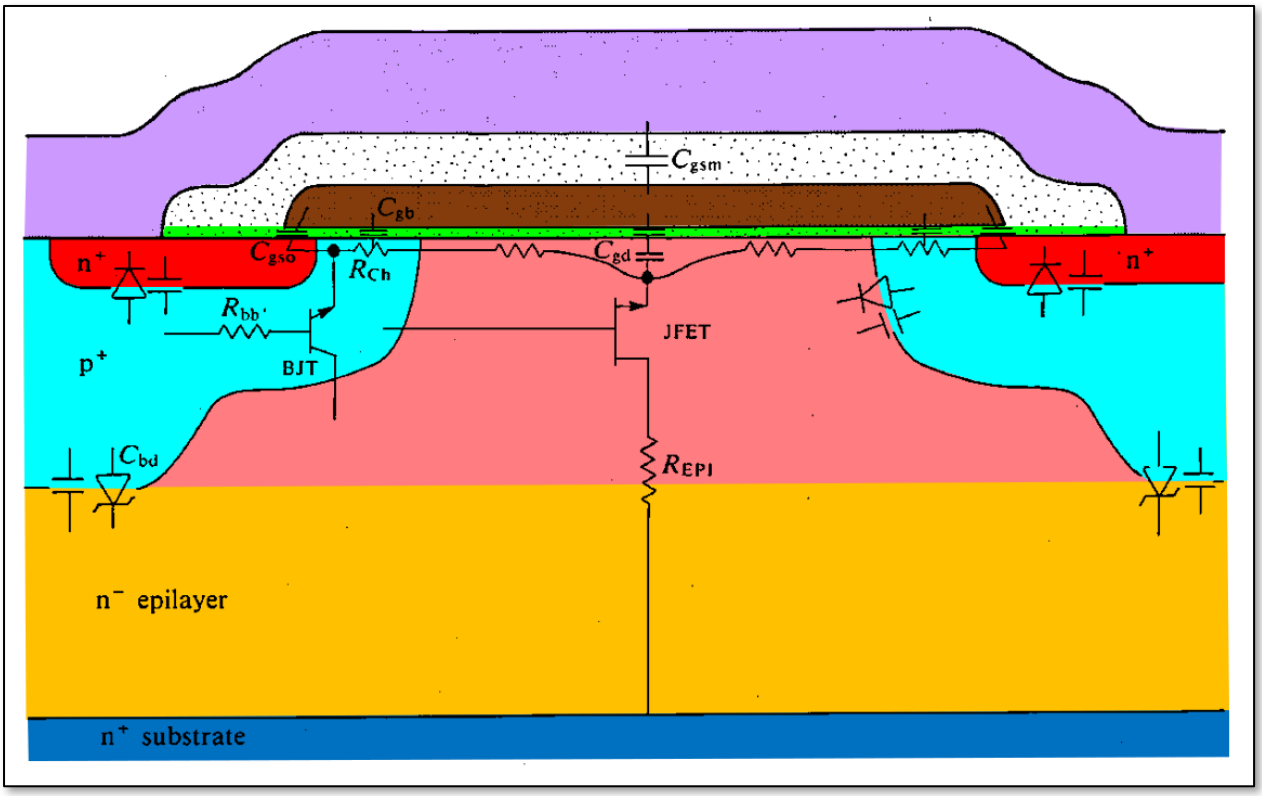
The term "double-diffused" derives from a manufacturing technique commonly used to form the n+ source regions and the p-type body region. *See, e.g.*, EX1019, 13–14; EX1005, 2:35–41. The p-type body region is often referred to as "p-type wells" or "p-base regions." *See, e.g.*, EX1019, 146; EX1005, 2:35, Figure 1. EX1035, ¶31.

In *Grant*'s Figure 1.11 and *Baliga*'s Figure 1 above, the source regions are annotated in red, p-type body regions in cyan, gate in brown, gate oxide in green, and source contacts in lavender. The drain region (yellow) comprises the substrate (blue) and the epilayer (orange). Electrons flow from the source to the drain through the channels formed in the p-type wells, the epilayer, and the substrate. The epilayer is often referred to as the "drift region." *See, e.g.*, EX1019, 74. EX1035, ¶32.

C. On-Resistance

According to *Grant*, "minimization of the ON-state voltage drop is an important consideration in power devices." EX1019, 18. This ON-state voltage drop depends on the "ON-state drain-source resistance, $R_{DS(on)}$"—also known as the "on-resistance." *Id.* U.S. Patent No. 6,413,822 ("*Williams*") explains that "[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents." EX1004, 1:50–52. *Williams* also discloses topological configurations that minimize the source contact resistance. *See* EX1004, 10:17–18; 16:28–35. EX1035, ¶¶33–34, 36.

Grant describes and illustrates in Figure 3.15 (below) the existence of a parasitic "n-channel junction field-effect transistor (JFET) that forms in the epilayer, in between the channel diffusions." EX1019, 80–81. "The JFET action occurs in the region between the p diffusions." *Id*., 81. Accordingly, this region is typically referred to as the "JFET region." *See, e.g.*, EX1033, H4.5.2; EX1029, FIG. 1, ¶2; EX1003, ¶44. The JFET region is annotated in salmon in *Grant*'s Figure 3.15 below. EX1035, ¶35.

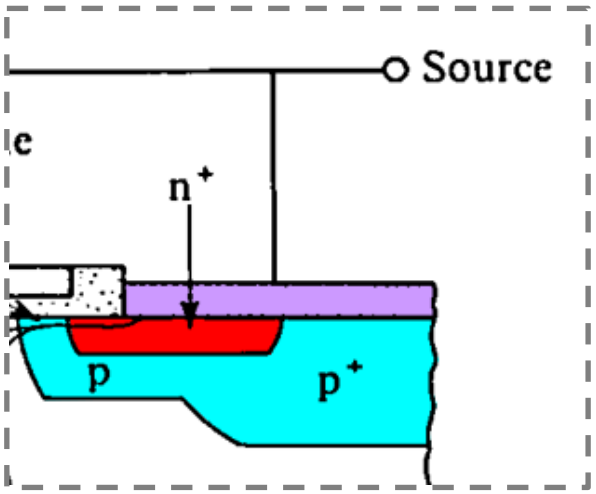


EX1019, Figure 3.15 (annotated)

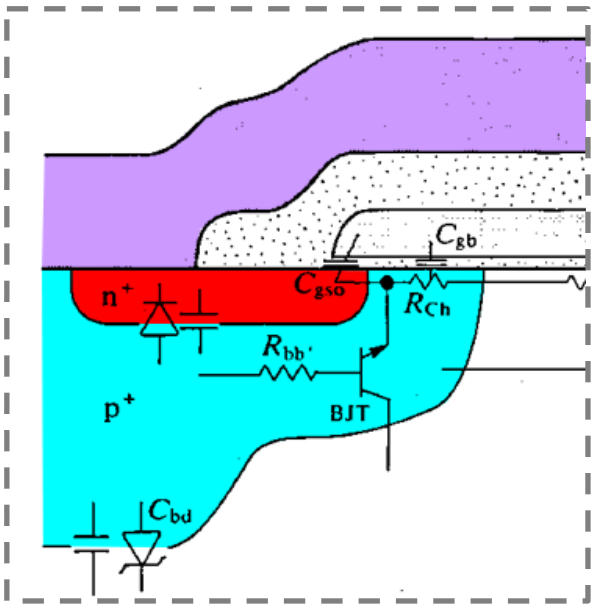
D. Unwanted Activation of Parasitic Components

Grant explains that an "npn bipolar junction transistor (BJT) formed between the source, the body, and the drain." EX1019, 81. The parasitic BJT "may be activated, and this can seriously degrade the overall performance of the MOSFET." *Id.*; *see also* EX1007, ¶¶6–7. Unwanted activation of parasitic components is sometimes known as "latch up." To prevent unwanted turn on, "the P-base region is short-circuited to the N^+-emitter region by the source metallization . . ." EX1032, 266; *see also* EX1004, 6:8–14. As shown below, it was well-known to short the p-type body or p-base region (*i.e.*, the base of the parasitic BJT; cyan) to the source

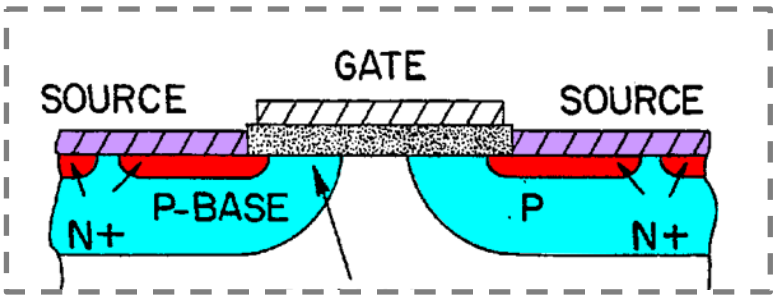
region (*i.e.*, the emitter of the parasitic BJT; red) by an overlying and contacting source metallization (lavender) to keep the parasitic BJT inactive. *See, e.g.*, EX1019, 2, 80 (Figures 1.11 and 3.15); EX1005, Figure 1. EX1035, ¶¶37–38.



EX1019, Figure 1.11
(excerpted and annotated)



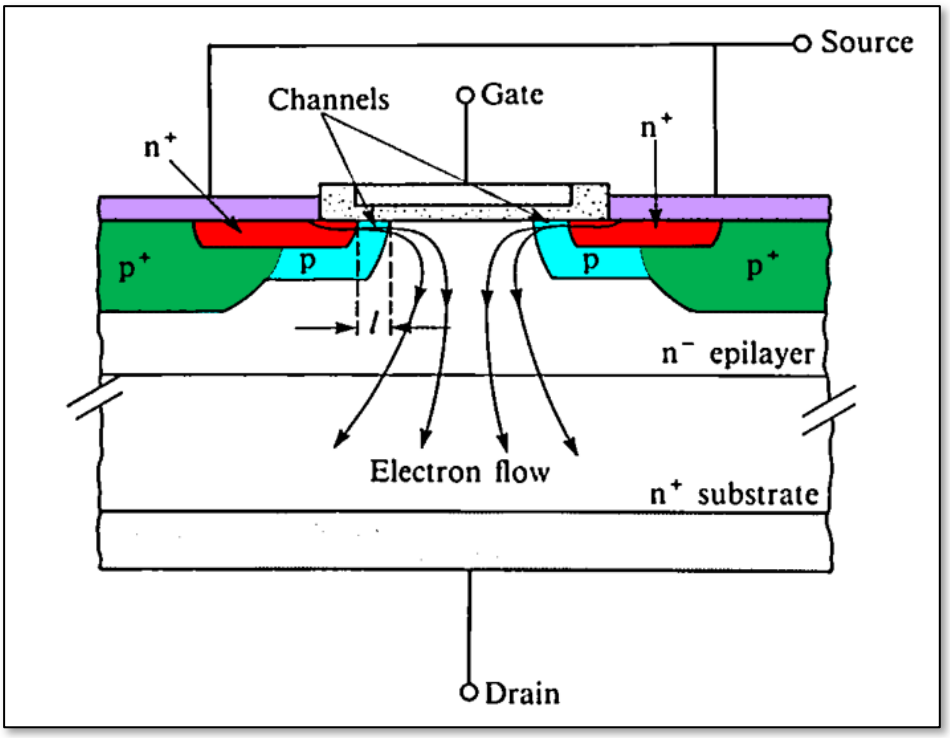
EX1019, Figure 3.15
(excerpted and annotated)



EX1005, FIG. 1(excerpted and annotated)

Grant further explains that current flowing through the resistance $R_{bb'}$ (*see Grant*'s Figure 3.15, above) at the base of the parasitic BJT causes a voltage drop which, if it exceeds about 0.6 V, "will initiate transistor action in the parasitic BJT." EX1019, 87. To reduce resistance and minimize voltage drop, *Grant* explains "[t]he

use of the p+ diffusion to connect the body region back to the source contact can be seen to be an important part of the VDMOS FET design." *Id.*, 90; *see also id.*, 2, 16 (Figures 1.11 and 1.13(a)). "It reduces $R_{bb'}$ . . ." *Id.*, 90. Thus, a MOSFET may be ruggedized against inadvertent activation of the parasitic BJT by having p+ diffusion in the p-type body region. *See also* EX1004, 16:32–34; EX1021, 5:28–30. The p+ diffusions of *Grant*'s Figure 1.11 below are annotated in dark green. EX1035, ¶39.



EX1019, Figure 1.11 (annotated)

E. Silicon Carbide (SiC)

Historically, power MOSFETs were fabricated using silicon. By the early 1990s, silicon carbide (SiC) was known to be particularly well suited for use in such devices. EX1005, 4:22–27. SiC was known to allow SiC "power devices to operate

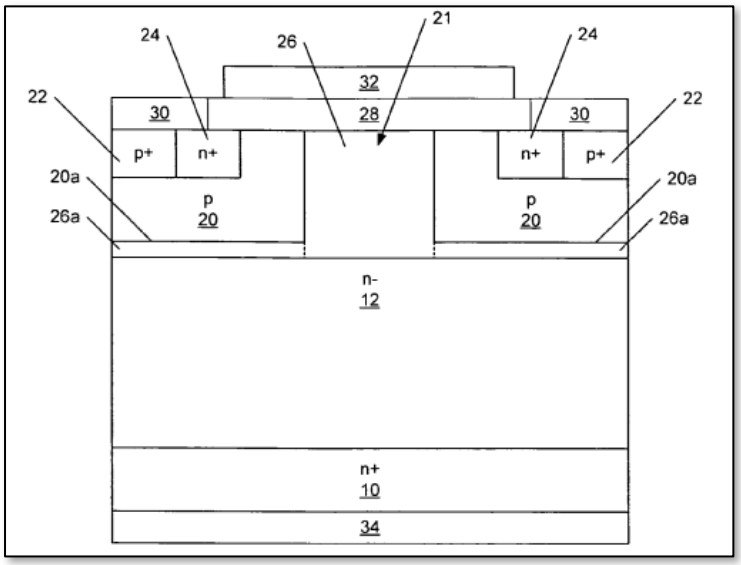
at higher temperatures, higher power levels and with lower specific on resistance than conventional silicon based power devices." *Id.*, 4:27–34; *see also* U.S. Patent No. 5,510,281 ("*Ghezzo*") (EX1021), 1:52–56. EX1035, ¶40.

Moreover, *Baliga* teaches that "power MOSFET such as the above described DMOSFET . . . can be readily translated into SiC using known manufacturing techniques," *e.g.*, by using higher temperature, and longer, diffusions to compensate for the lower diffusion coefficient in SiC. EX1005, 4:35–43. *Ghezzo*, which was filed in 1995, further teaches that "[a] method of implementing vertical power SiC transistor is to replace the conventional double-diffusion with an edge-shifted ***double ion implantation*** sequence to overcome the problem of very small dopant diffusivity in SiC"[2] and that "[t]he channel is formed by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) to form the base and source regions, respectively." EX1021, 1:56–63. SiC power MOSFETs are sometimes referred to as "double-implanted" MOSFETs to distinguish the "double-diffused" fabrication technique used in silicon. EX1035, ¶41.

[2] Unless otherwise noted, all emphasis has been added.

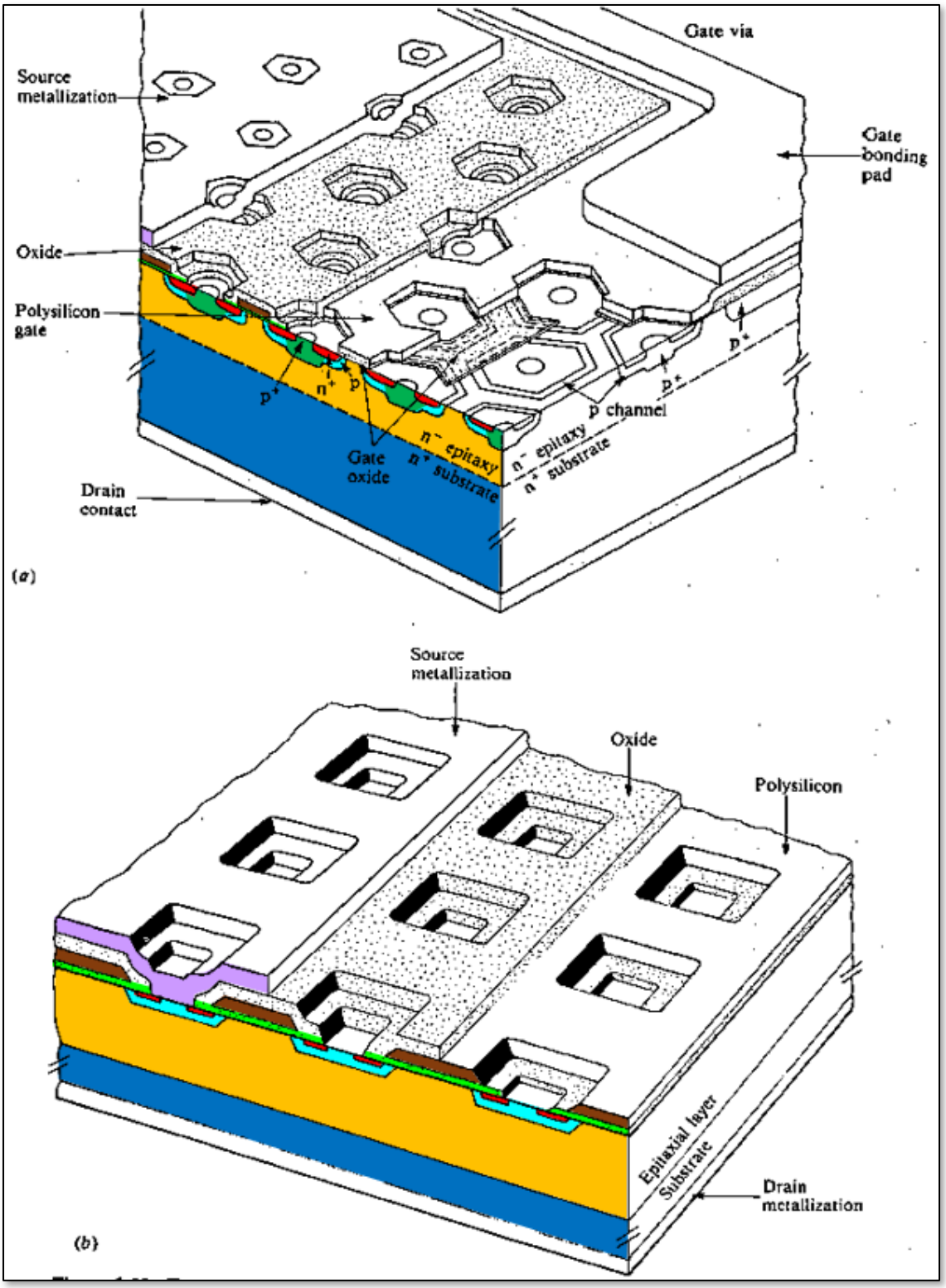
F. Visualizing Semiconductor Structures

Prior art references conventionally depict a unit cell of a power MOSFET in cross-section (*e.g.*, *Grant*'s Figure 1.11 and *Baliga*'s Figure 1). U.S. Patent Application Publication No. 2004/0119076 ("*Ryu*") (EX1003) also shows a cross section of a unit cell of a MOSFET in Figure 2A. *See* EX1003, ¶51. EX1035, ¶42.



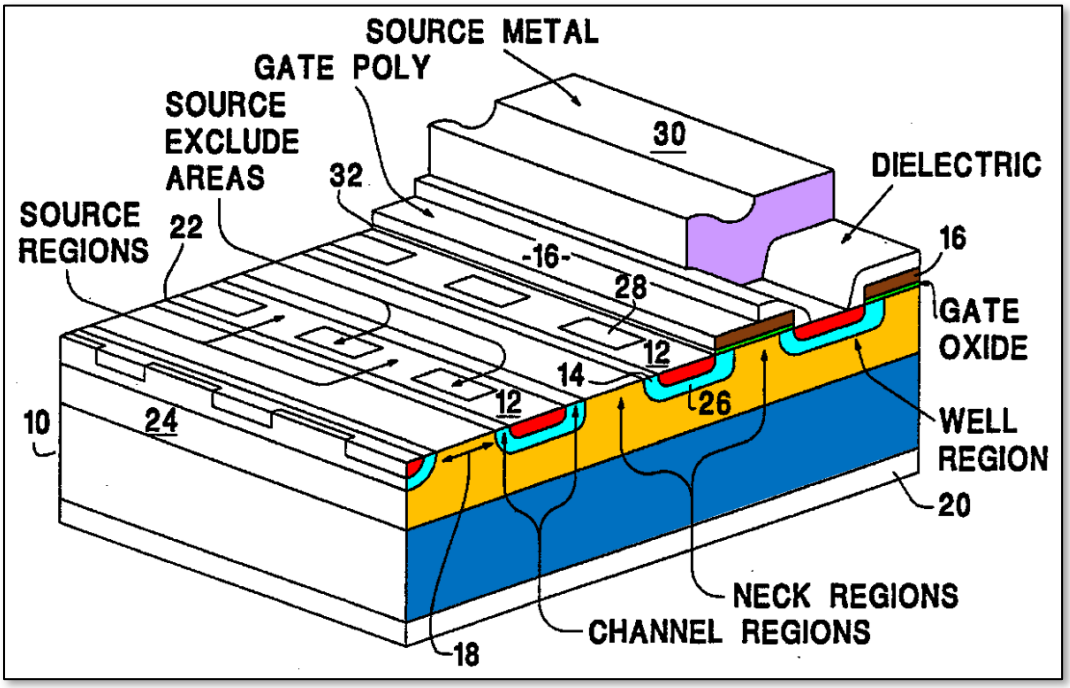
EX1003, FIG. 2A.

MOSFETs may have cross sections that are the same as or similar to *Grant*'s Figure 1.11, *Baliga*'s Figure 1, and *Ryu*'s Figure 2A, yet have different—though all well-known—three-dimensional hexagonal, square, circular, linear, or triangular cellular structures. *See* EX1032, 338–339; *id*., Figures 6.55 and 6.56; EX1019, 15–17, 70–73, 455–457. For example, *Grant*'s Figure 1.13 (below) illustrates two cellular structures—hexagonal and square—that have similar cross sections. EX1035, ¶43.



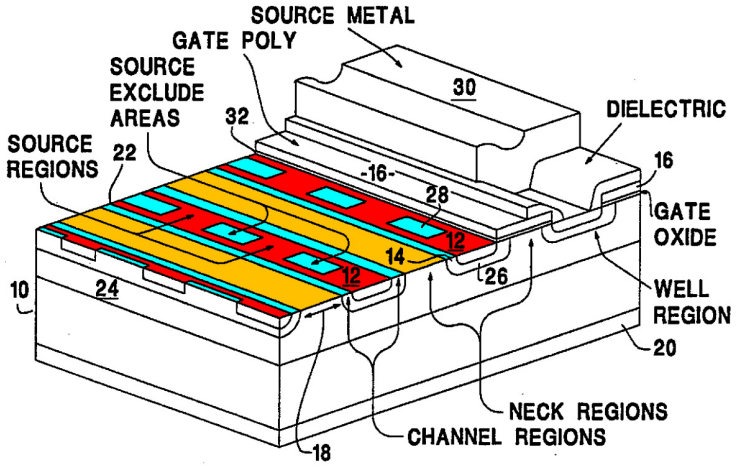
EX1019, Figure 1.13 (annotated)

Figure 1 (below) of U.S. Patent No. 5,317,184 ("*Rexer*") (EX1015) shows a three-dimensional linear cellular design of a MOSFET that also has a similar cross section to those in *Grant*'s Figure 1.13. EX1035, ¶44.

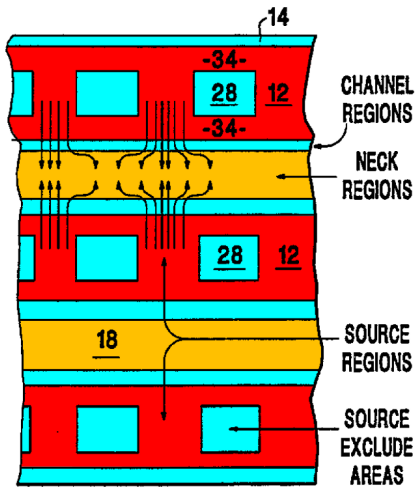


EX1015, FIG. 1 (annotated)

Top or plan views of power MOSFETs may also be shown. For example, *Rexer* illustrates, in Figure 2, a partial plan view of the surface 22 of its MOSFET of Figure 1. EX1015, 1:43–45, 2:34–36. In *Rexer*'s Figure 2, the linear cellular structure is shown extending left-to-right in the plan view. EX1035, ¶45.

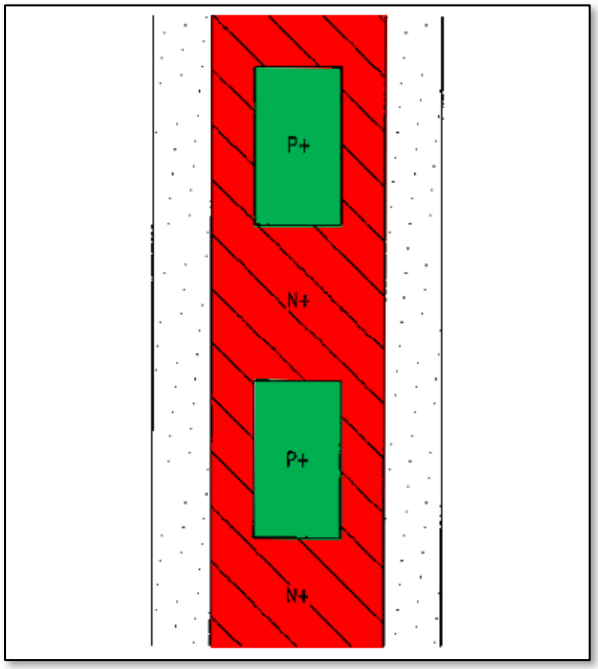


EX1015, FIG. 1 (annotated)



EX1015, FIG. 2 (annotated)

Williams shows top views of other known MOSFET features such as a linear cellular structure extending top-to-bottom in Figure 19E. EX1035, ¶46.



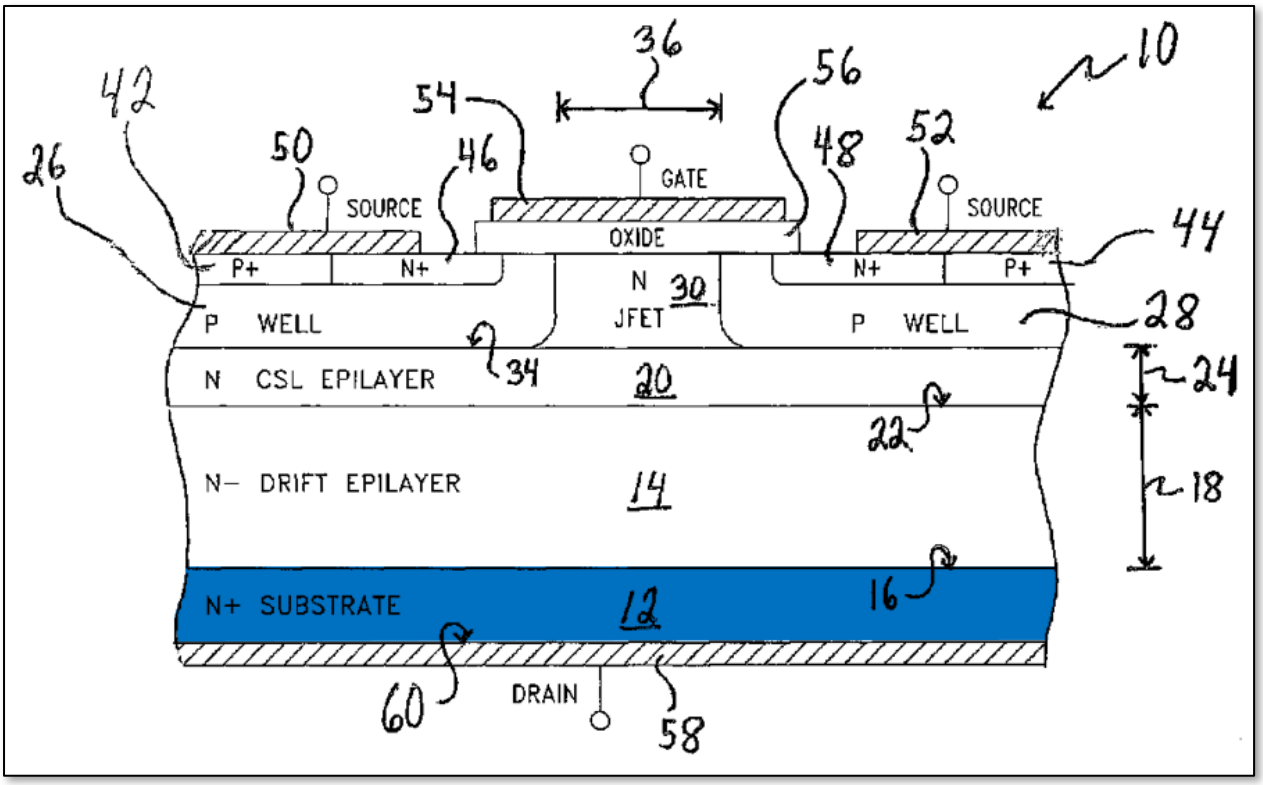
EX1004, FIG. 19E

The relationships between cross-sectional, perspective, and top views of MOSFETs were well known. A POSITA would have understood that, if a cross-sectional view of a unit cell of a MOSFET like shown in *Ryu*'s Figure 2A were of a linear cellular design like in *Rexer*, then *Ryu*'s cellular structure would extend perpendicular to the page. Similarly, a POSITA would have recognized that a top view like *Williams*'s Figure 19E would extend in the same longitudinal direction as the top side of *Rexer*'s three-dimensional MOSFET. EX1035, ¶47.

VII. THE '633 PATENT

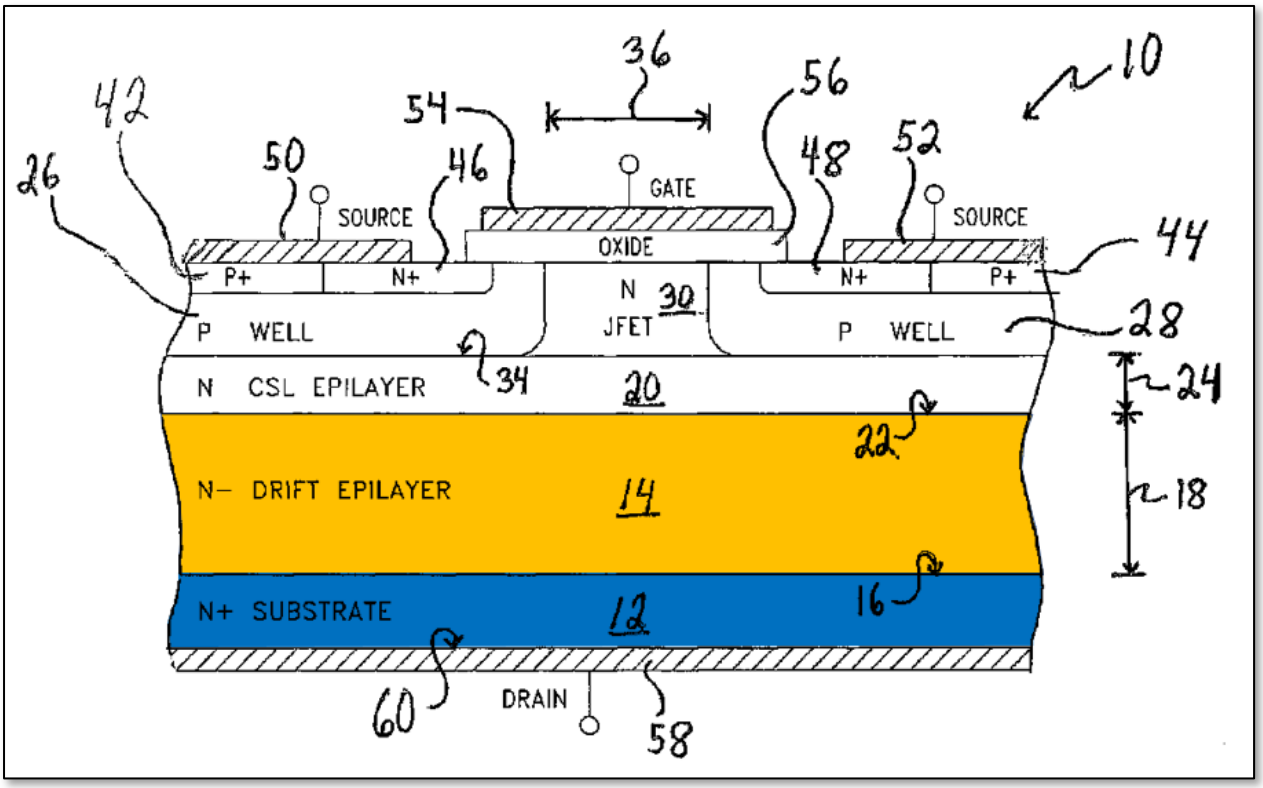
A. Alleged Invention

The '633 patent is directed to semiconductor devices for high-voltage power applications, in particular a "vertical double-implanted metal-oxide semiconductor field-effect transistor." EX1001, 1:12-14, 3:7–8, 4:4-9, Figure 1. As the '633 patent's Figure 1 shows, the semiconductor device 10 includes a **substrate 12** (blue below) formed from silicon-carbide and doped with N-type impurity to an "N+" concentration. EX1001, 4:4–13. EX1035, ¶48.



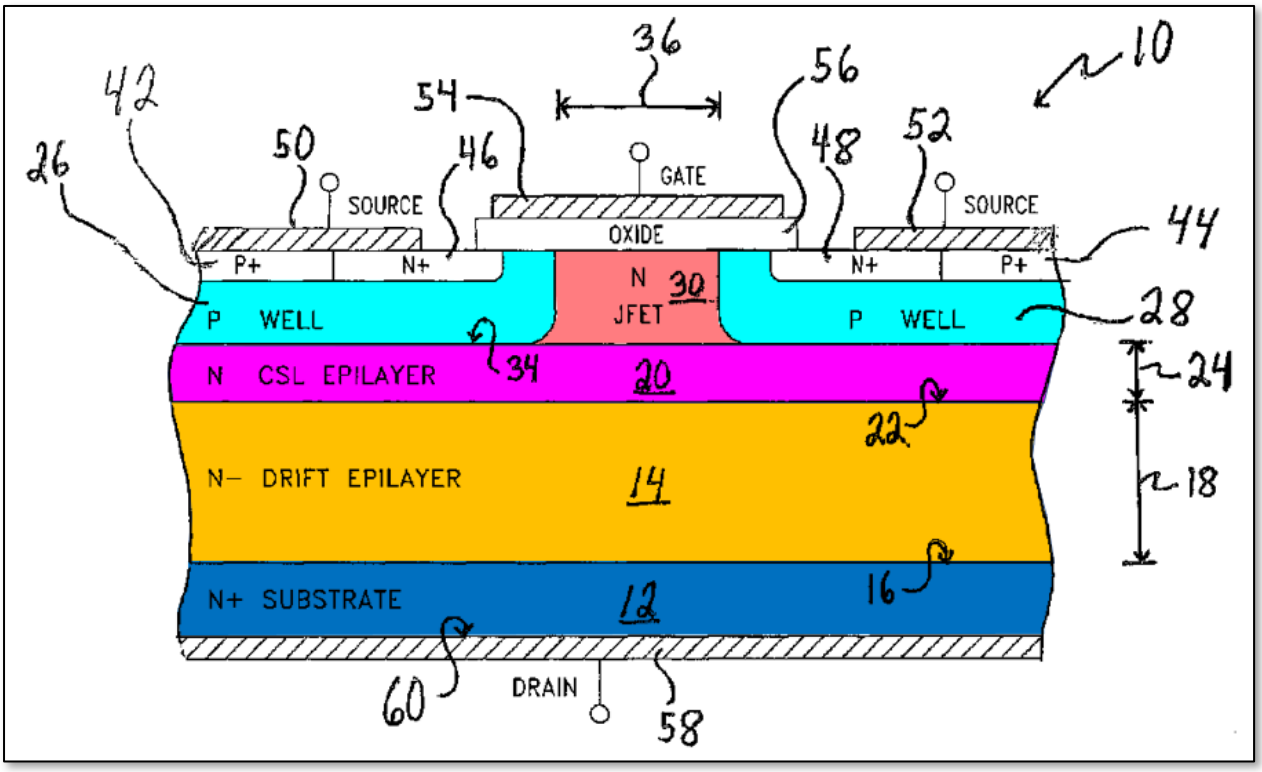
EX1001, FIG. 1 (annotated)

The semiconductor device 10 also includes a **drift layer 14** (orange below) formed on the **substrate 12**. *Id.*, 4:20–21. The **drift layer 14** may be epitaxially grown and formed of silicon-carbide, and doped with N-type impurities to an "N–" concentration. *Id.*, 4:35–41. EX1035, ¶49.



EX1001, FIG. 1 (annotated)

Formed on **drift layer 14** is a **current semiconductor spreading layer (CSL) 20** (magenta below). *Id.*, 5:1–3. The device 10 also includes two doped semiconductor **wells or base regions 26, 28** (cyan) formed above the **CSL 20** and a **junction field-effect transistor (JFET) region 30** (salmon) formed between the **wells 26 and 28**. *Id.*, 5:23–26. EX1035, ¶50.



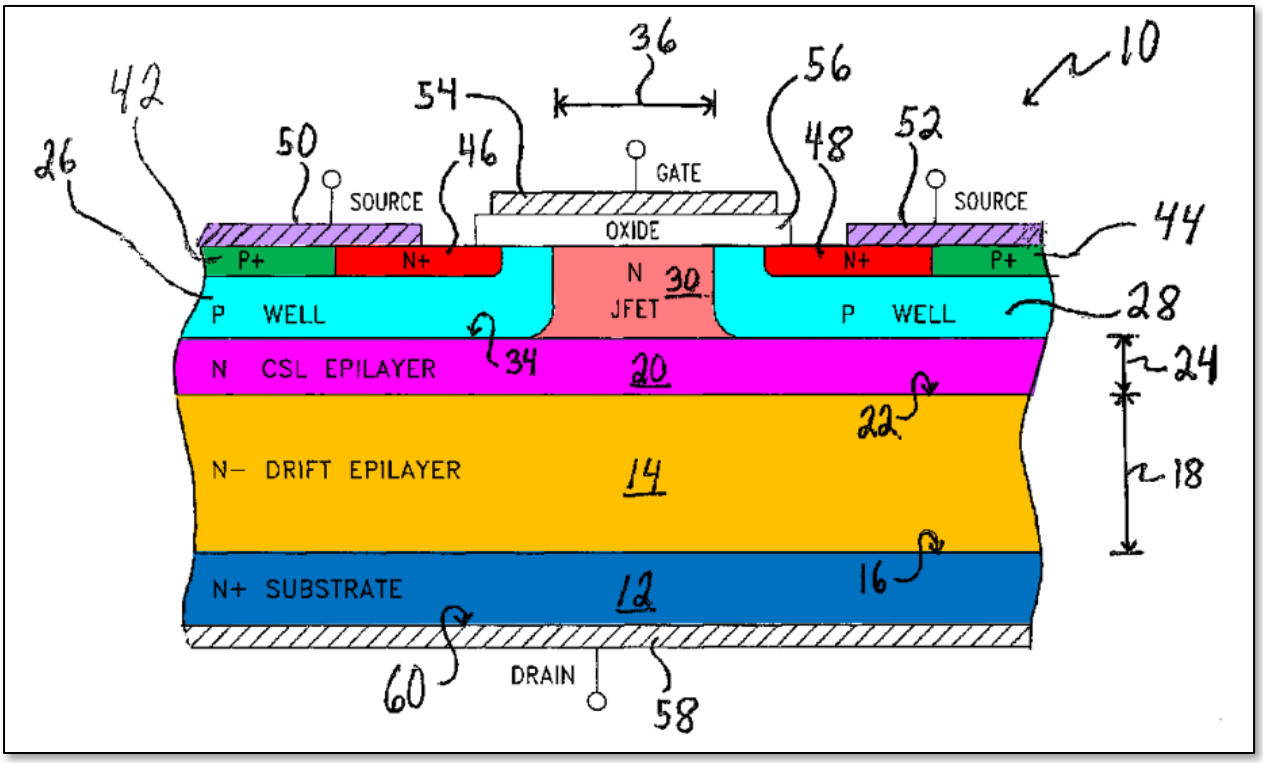
EX1001, FIG. 1 (annotated)

The '633 describes two embodiments for forming the **JFET region 30** such that it has similar "N" doping concentrations to the **CSL 20**. *Id.*, 5:54–56, Figure 1 (which labels both **JFET region 30** and **CSL 20** as "N"). In one embodiment, the **JFET region 30** may be formed by growing an extra-thick **CSL 20** and implanting the **wells 26, 28**. *Id.*, 5:56–60. In another embodiment, after the **CSL 20** is formed on the **drift layer [14]**, an additional epitaxial layer may be formed on the **CSL 20** and the **wells 26, 28** may be implanted in the additional epitaxial layer. *Id.*, 5:64–6:3. While the challenged claims cover both embodiments, they do not require a

two-step process of growing an additional epitaxial layer after forming the **CSL 20**. EX1035, ¶51.

According to the '633 patent, "forming a **JFET region 30** with a doping concentration that is greater than the doping concentration of the **drift layer 14**," and fabricating the **JFET region 30** to have a width 36 of "three micrometers or less . . . may reduce the specific on-resistance of the semiconductor device 10." EX1001, 6:16–26; *cf.* EX1019, 83–84 ("Increasing the donor doping concentration in the drain throats . . . has two beneficial effects . . . ***cell size can be reduced*** and . . . ***lower $R_{DS(on)}$ can be realized***."). EX1035, ¶52.

The semiconductor device 10 also includes N-type **source regions 46, 48** (red below) "defined in the P **wells 26 and 28**, respectively." EX1001, 6:63–66. P-type **base electrode regions 42, 44** (dark green below and alternately referred to as "base contact regions" in the '633 patent specification) are located beside **source regions 46, 48**, respectively. *Id.*, 6:66–7:2; 7:30. Metallic **source electrodes 50, 52** (lavender below) are formed over the **source regions 46, 48**, respectively, and also extend over the **base electrode regions 42, 44**. *Id.*, 7:4-6. EX1035, ¶53.

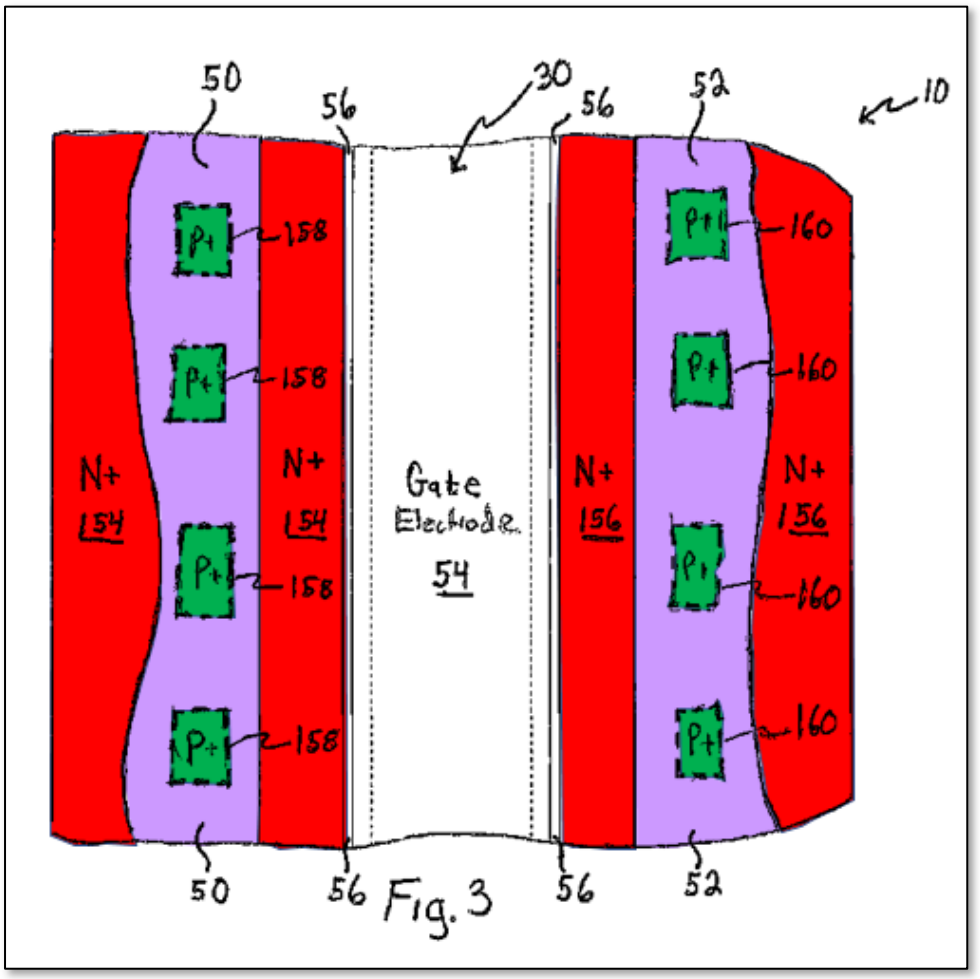


EX1001, FIG. 1 (annotated)

To address potential misalignment between the source regions, base contact regions, and the source electrodes, the '633 patent describes embodiments having source regions that each include "a plurality of base contact regions" arranged to increase "the tolerance to manufacturing variability." *Id.*, 7:52–8:6. EX1035, ¶54.

Figure 3 shows one embodiment where "the **base contact regions 158, 160** are embodied as small 'islands' or regions within the larger **source regions 154, 156**." EX1001, 7:57–59. The annotated Figure 3 below shows the "islands" of **base contact regions 158, 160** as if they are visible in the plan (or top) view; however, it is understood that **source electrodes 50, 52** would cover **base contact regions 158,**

160 in the physical device such that the "islands" would not be visible in the plan view (as denoted by dashed lines in the original Figure 3). EX1035, ¶55.



EX1001, FIG. 3 (annotated)

Figure 4 shows another embodiment where **source regions 188, 190** and **base contact regions 184, 186** are embodied as alternating strips. *Id.*, 8:7–11. The "strip" **base contact regions 184, 186** are annotated in light green to distinguish the "island" **base contact regions 158, 160** (dark green) in Figure 3. However, it is understood that the **base contact regions 184, 186** and the **base contact regions 158, 160** have

the same functionality, namely providing a low resistance ohmic contact to the **wells 26 and 28**. *See* Section VI.D. The **source electrodes 50, 52** are illustrated as covering the midsection of the alternating strips of **source regions 188, 190** and **base contact regions 184, 186**; however, it is understood that **source electrodes 50, 52** would be wider than illustrated. EX1035, ¶56.

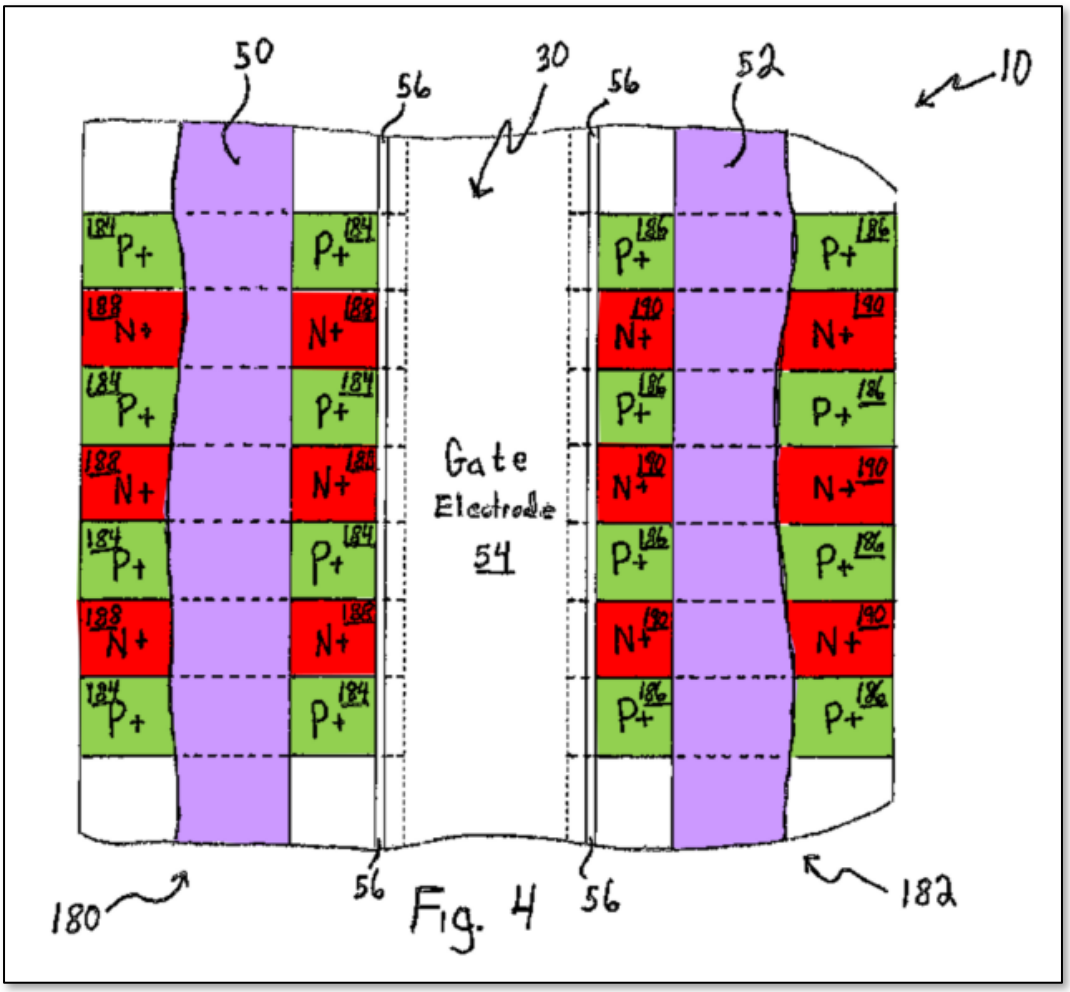


Fig. 4

EX1001, FIG. 4 (annotated)

As demonstrated below, the challenged claims were well-known in the art before the '633 patent's priority date. EX1035, ¶57.

B. Prosecution History

The Examiner issued a non-final Office Action on April 4, 2007, rejecting all originally-filed claims 1–23[3] over several prior art references. EX1008, 2–15. In response, Applicant amended independent claims 1 and 12 to require a silicon-carbide substrate, and claims 12 and 17 to be respectively directed to specific topological configurations of the '633 patent's Figures 3 and 4. EX1009, 2–6. Applicant argued that, because "Ono and Zeng are directed toward MOSFET device having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices, . . . it is clear that no one of ordinary skill in the art would combine Ono or Zeng with Kumar." *Id.*, 9–10. As explained below, Petitioner disagrees with Applicant's argument. A POSITA would have been motivated to modify prior art SiC references based on teachings regarding silicon structures. *See* EX1005, 4:22–38; EX1035, ¶¶58-59.

Correctly unpersuaded by Applicant's argument, the Examiner issued a final Office Action, rejecting all claims, stating "Ono and Zeng disclose ***the structure of the DMOS device*** and Kumar teaches the alternative of silicon-carbide with its known advantages[,] one of ordinary skill would indeed consider whether their

[3] Pending independent claims 1, 12, and 17 correspond to issued claims 1, 9, and 12, respectively.

particular problem would call for silicon-carbide." EX1010, 12. Applicant responded with similar arguments, but also further amended claims 12 and 17. *See* EX1011, 2–9; EX1035, ¶60.

The Examiner rejected claim 1, maintaining that a POSITA would combine silicon and SiC references, and allowed claims 12 and 17. EX1012, 2, 9–10. The Examiner also indicated the allowability of claim 1's dependent claim 11, which was directed to the same topological configuration as claim 17. EX1012, 9. Thereafter, Applicant amended claim 1 to include the subject matter of claim 11. EX1013, 2, 8. The Examiner subsequently issued a Notice of Allowance. EX1014, 2; EX1035, ¶61.

The Examiner did not have the benefit of *Ryu* and *Williams*, which are not of record. As this Petition demonstrates, *Ryu* and *Williams* render obvious the allegedly inventive features of the '633 patent, including the topological configurations recited by issued claims 1 and 12 and their dependents. EX1035, ¶62.

VIII. PRIOR ART PATENTS AND PUBLICATIONS

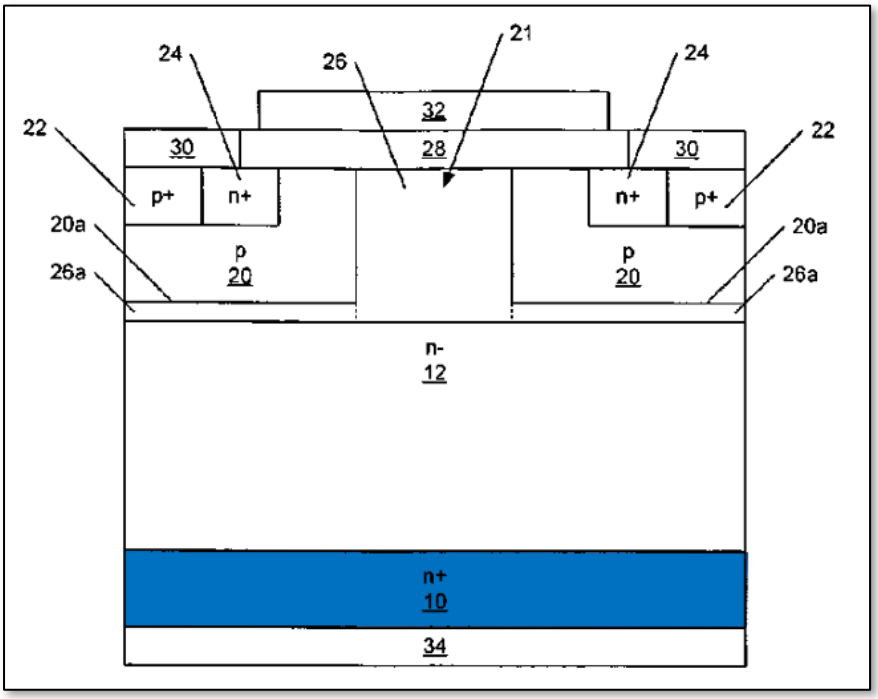
The following references are pertinent to the ground of unpatentability:

A. *Ryu*

U.S. Patent Application Publication No. 2004/0119076 to Ryu ("*Ryu*") (EX1003) was filed on October 30, 2003 and published on June 24, 2004. *Ryu* is prior art at least under 35 U.S.C. §§ 102(a) and 102(e). *Ryu* is not art-of-record.

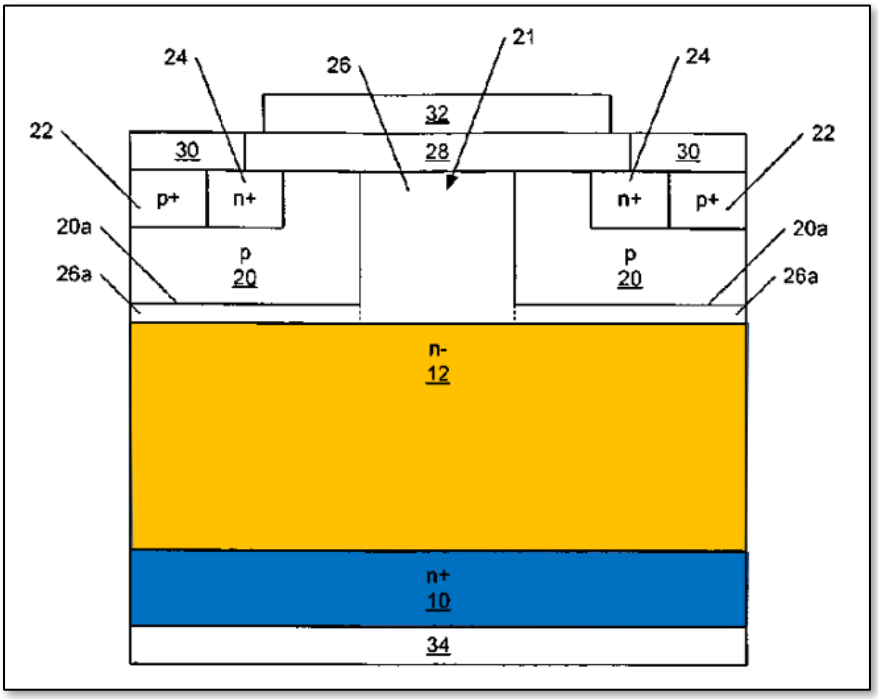
Like the '633 patent, *Ryu* relates to "semiconductor devices . . . and, more particularly, to silicon carbide (SiC) metal-oxide semiconductor field effect transistors (MOSFETs)." EX1003, ¶3. Also like the '633 patent, *Ryu*'s embodiments of SiC MOSFETs "may reduce on-state resistance." *Id.*, ¶¶39, 64, 65. EX1035, ¶64.

Ryu's Figure 2A (below) shows a cross-sectional view of an embodiment of *Ryu*'s vertical MOSFET, which is strikingly similar to the '633 patent's MOSFET. EX1003, ¶¶28, 40. In *Ryu*'s Figure 2A, **layer 10** (blue below) may be a substrate made of SiC and doped to an "n+" concentration. *See id.*, ¶40. EX1035, ¶65.



EX1003, FIG. 2A (annotated)

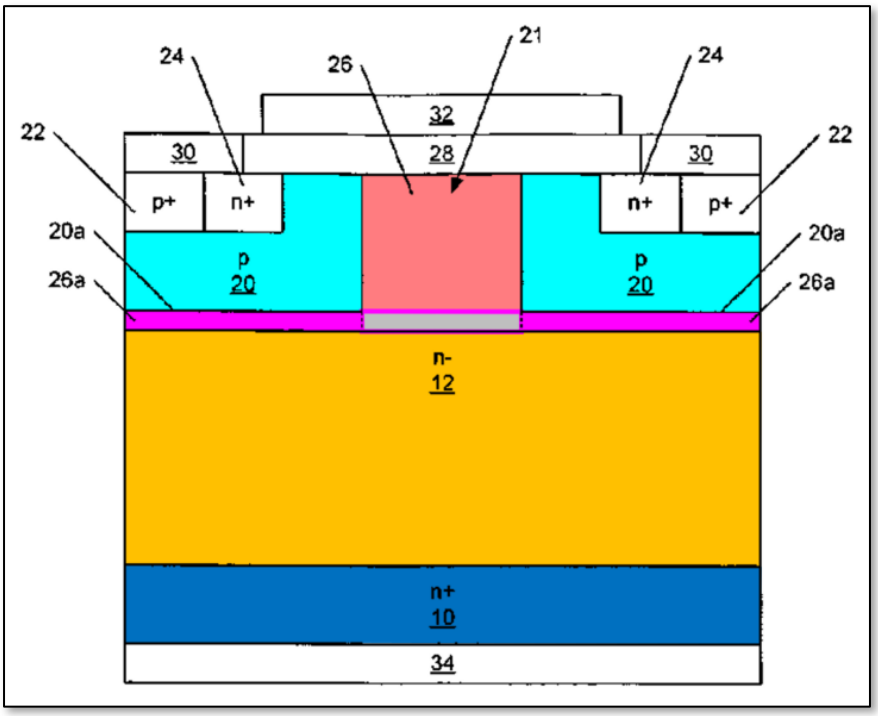
Ryu's MOSFET further includes a **drift layer 12** (orange below) on the substrate **layer 10**. *Id.*, ¶40. The **drift layer 12** may be an epitaxial layer of SiC and doped to an "n−" concentration. *Id.* EX1035, ¶66.



EX1003, FIG. 2A (annotated)

Ryu discloses that "[a] region of higher carrier concentration n-type silicon carbide 26 is provided on the **drift layer 12**" and "p-wells 20 are implanted so as to extend into but not through the region 26 such that a region of higher carrier concentration n-type silicon carbide 26a is provided between a floor 20a of the p-wells 20 and the **drift layer 12**." *Id.*, ¶¶41–42. Like the '633 patent, *Ryu* refers to the gap between the p-wells 20 as the "JFET region 21." *Id.*, ¶44; *cf.* EX1001, 5:25–26 ("a junction field-effect transistor (JFET) region 30 formed between the wells 26

and 28"). A POSITA would have appreciated that the strip between regions 26a and below the JFET region 21 promotes lateral current spreading into the regions 26a and thus, together with the regions 26a, forms a current spreading layer. *See* Section X. Below, *Ryu*'s **p-wells 20** are annotated in cyan, **regions 26a** in magenta, and **JFET region 21** in salmon. The **strip** between **regions 26a** and below the **JFET region 21** is colored in grey and outlined in magenta. EX1035, ¶67.

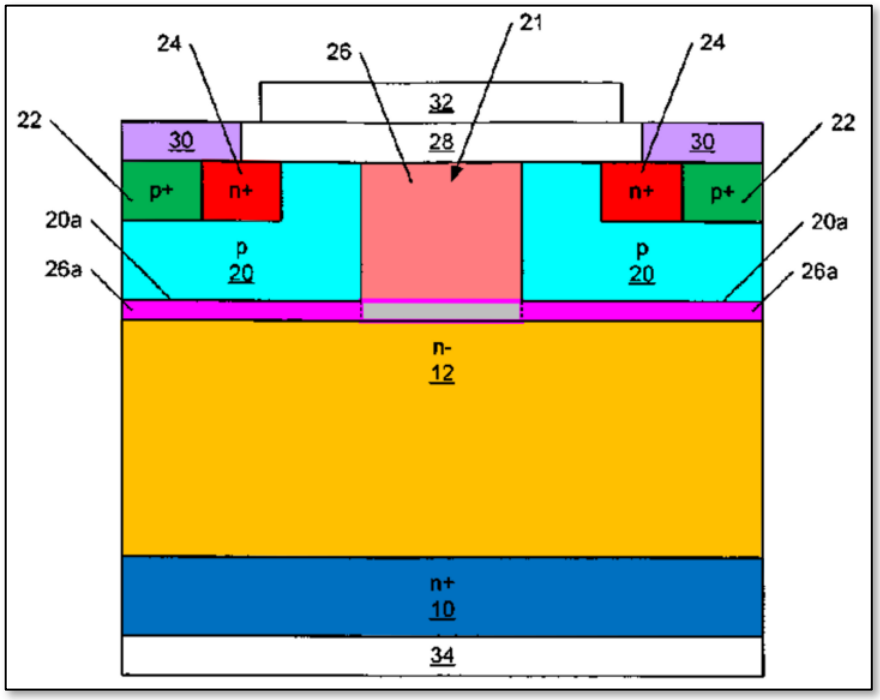


EX1003, FIG. 2A (annotated)

Like the '633 patent, *Ryu* explains that "the gap 21 [(*i.e.*, the **JFET region 21**)] between the **p-wells 20** has a higher carrier concentration than the **drift layer 12**." *Id.*, ¶42. According to *Ryu*, "if the gap is too narrow, the resistance of the

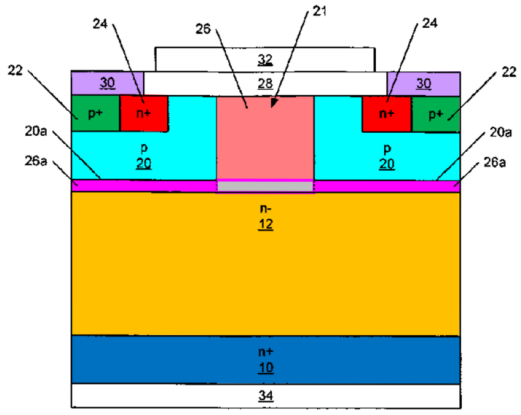
JFET region 21 may become very high." *Id.*, ¶44. Therefore, *Ryu* discloses that "gaps of from about 1 μm to about 10 μm are preferred." *Id.* EX1035, ¶68.

Ryu's MOSFET also includes **n+ regions 24** (red) and **p+ regions 22** (green) disposed within the **p-wells 20**. EX1003, ¶45. The **n+ regions 24** are doped to a "n+" concentration. *Id.*, ¶¶6, 45, Figure 1. The **p+ regions 22** are adjacent to the **n+ regions 24** and formed by implanting p-type impurities to a "p+" concentration. *Id.*, ¶55. *Ryu* further discloses **source contacts 30** (lavender) "to provide an ohmic contact to both the **p+ regions 22** and the **n+ regions 24**." EX1003, ¶47. EX1035, ¶69.

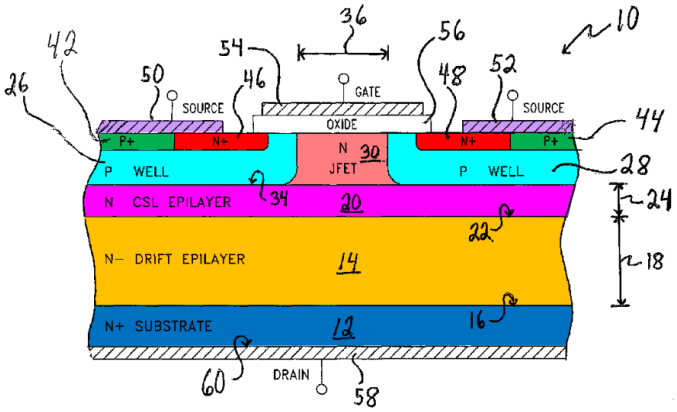


EX1003, FIG. 2A (annotated)

Comparing *Ryu*'s Figure 2A with the '633 patent's Figure 1 reveals that *Ryu* discloses the same relevant semiconductor structure as the '633 patent. EX1035, ¶70.



EX1003, FIG. 2A (annotated)



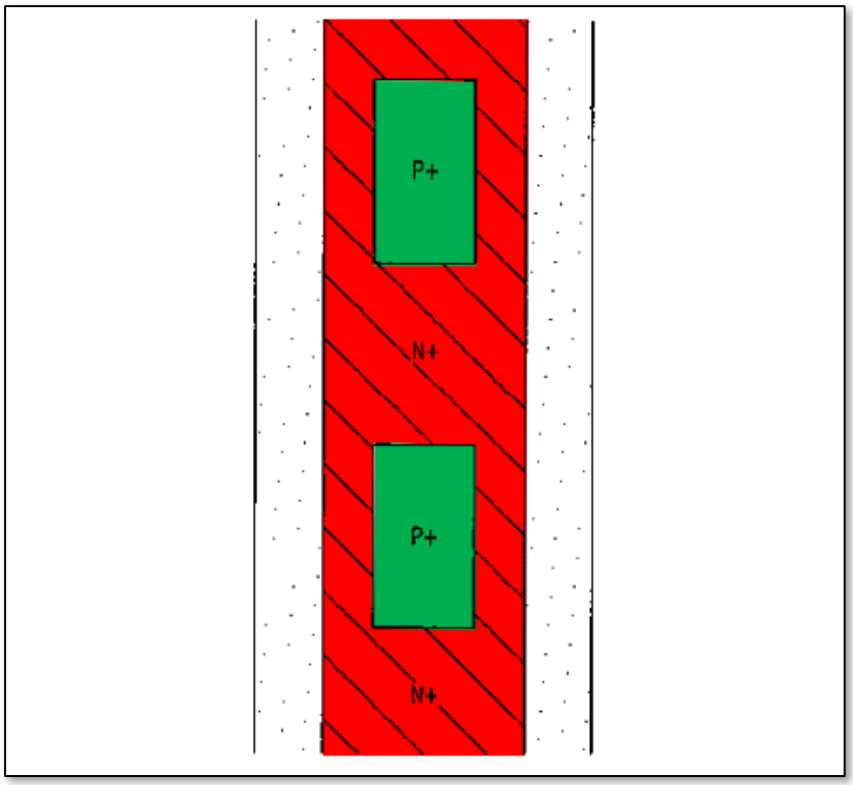
EX1001, FIG. 1 (annotated)

B. *Williams*

U.S. Patent No. 6,413,822 ("*Williams*") (EX1004) issued on July 2, 2002 and is prior art under at least 35 U.S.C. § 102(b). *Williams* is not art-of-record.

Like the '633 patent, *Williams* relates to vertical MOSFETs. *See, e.g.*, EX1004, 1:7–8, Figure 1. *Williams* discloses "plan views of various source-body designs" in Figures 19A–19F—including plan views just like those of the '633 patent—to "achieve the lowest possible resistance" by maximizing the area of the **N+ source regions** and/or to "suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device" (*i.e.*, prevent unwanted activation of the parasitic bipolar transistor) by maximizing the contact of the **P+ body contact regions** to the body region. *Id.*, 10:17–18; 16:28–35. EX1035, ¶71.

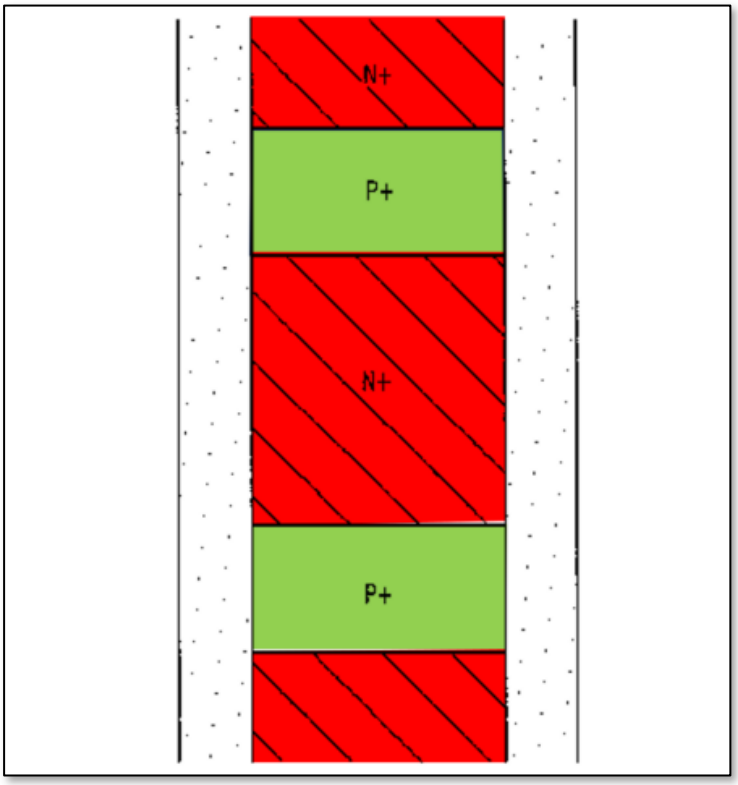
Like the '633 patent's source regions 154, 156 with "island" base contact regions 158, 160, *Williams* also discloses a continuous **N+ source region** (red below) with **P+ body contact windows** (dark green) in Figure 19E, reproduced below. EX1004, 10:23–24; EX1001, Figure 3. Such a source-body design provides "better **N+** contact resistance and less **P+** contact area (less rugged)." EX1004, 17:18–19. EX1035, ¶72.



EX1004, FIG. 19E (annotated)

In Figure 19D (below), *Williams* discloses a "'bamboo' ladder structure (alternating **N+** and **P+** regions)," like the alternating strips of source regions 188, 190 and base contact regions 184, 186 in the '633 patent. EX1004, 10:21–22;

EX1001, Figure 4. The bamboo or ladder structure "does not comprise the N+ contact resistance at all" given that "the N+ source is contacted along its length except for an occasional P+ strap." EX1004, 17:5–8. EX1035, ¶73.



EX1004, FIG. 19D (annotated)

IX. CLAIM CONSTRUCTION

During IPR, claims are construed according to the "*Phillips* standard." *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board need only construe the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015); *Nidec Motor Corp. v.*

Zhongshan Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, given the close correlation between the asserted prior art and the challenged claims of the '633 patent, the Board need not construe any terms to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their plain meaning (as would have been understood by a POSITA at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.[4] EX1035, ¶63.

X. SPECIFIC GROUND FOR UNPATENTABILITY

Under 37 C.F.R. § 42.104(b)(4)–(5), the following sections (confirmed in Dr. Subramanian's declaration, EX1035, ¶¶74–174) detail the ground of unpatentability, the limitations of challenged claims 1–8 and 12–15 of the '633 patent, and how these claims are obvious in view of the prior art. EX1035, ¶¶74–174.

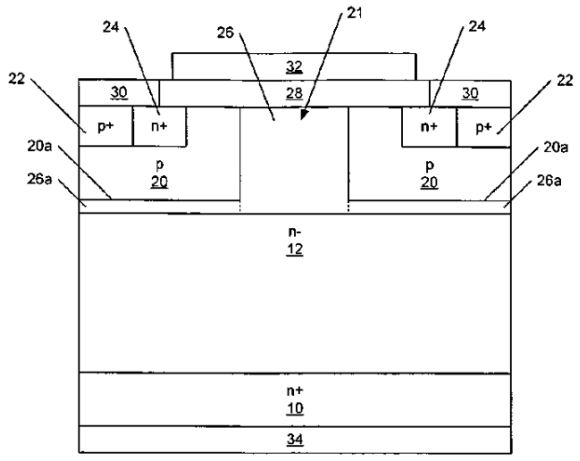
[4] Petitioner reserves all rights to raise claim construction and other arguments in this and other proceedings as relevant and appropriate.

A. Ground I: Claims 1–8 and 12–15 are Obvious Over *Ryu* in View of *Williams*

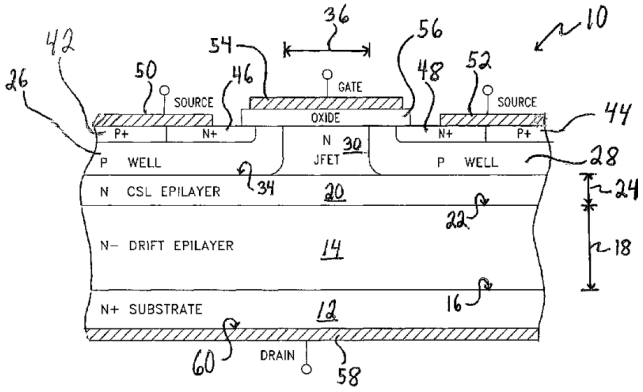
1. Claim 1

a) 1[preamble]: "A metal-oxide semiconductor field-effect transistor comprising:"

Regardless of whether the preamble is limiting, *Ryu* discloses it. *Ryu* discloses a metal-oxide semiconductor field-effect transistor (MOSFET). EX1003, ¶¶3, 28, 40. *Ryu* explicitly states that Figure 2A is a MOSFET. *Id.*, ¶40. *Ryu*'s Figure 2A is below, alongside the '633 patent's Figure 1 for comparison. EX1035, ¶76.



EX1003, FIG. 2A



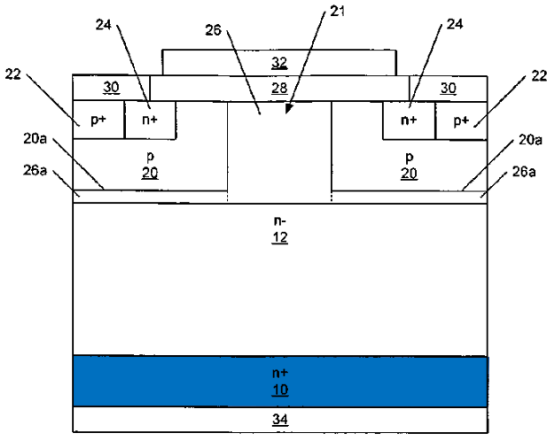
EX1001, FIG. 1

Ryu's MOSFET includes a gate contact 32 ("the gate contact is ***metal***"; EX1003, ¶13; *see also id.*, claims 10 and 41), over a gate oxide 28 ("The gate ***oxide*** may be thermally grown and may be a nitrided oxide and/or may be other oxides."; *id.*, ¶46), over a combination of silicon carbide (*i.e.*, a ***semiconductor***) layers 26, 12, and 10 (*id.*, ¶¶40–41), thereby creating a metal-oxide semiconductor device. EX1035, ¶77.

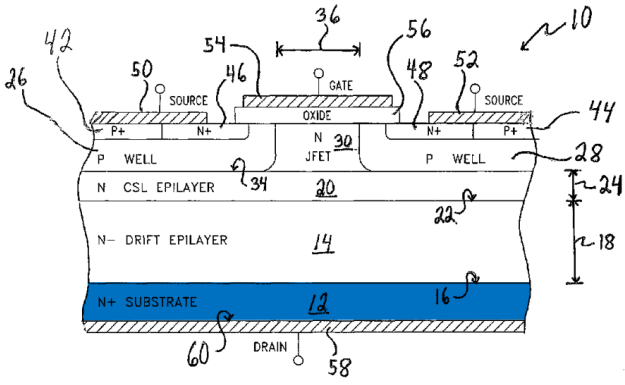
Therefore, *Ryu* discloses the preamble. *Id.*, ¶78.

b) 1[a]: "a silicon-carbide substrate having a first concentration of first type impurities;"

Ryu explains that its **layer 10** is made of silicon carbide. *See* Figures 2A, 2B, 3, and 4E. *Ryu* states that "…layer 12 of silicon carbide is on an optional n+ ***layer 10 of silicon carbide***." EX1003, ¶40. *Ryu* also explains that **layer 10** can be the substrate. *Id.*, ¶56 ("…***layer 10***, which may be formed by a backside implant of n-type impurities in a substrate or ***may be*** an epitaxial layer or ***the substrate itself***"). *Ryu*'s claims 13 and 23 also clearly disclose a silicon carbide substrate. *Id.*, claims 13 ("… comprising an n-type ***silicon carbide substrate***"), 23 ("… wherein the n-type silicon carbide layer comprises an n-type ***silicon carbide substrate***."). As shown below, *Ryu*'s **silicon carbide substrate 10** corresponds to the '633 patent's **silicon carbide substrate 12**. EX1035, ¶79.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

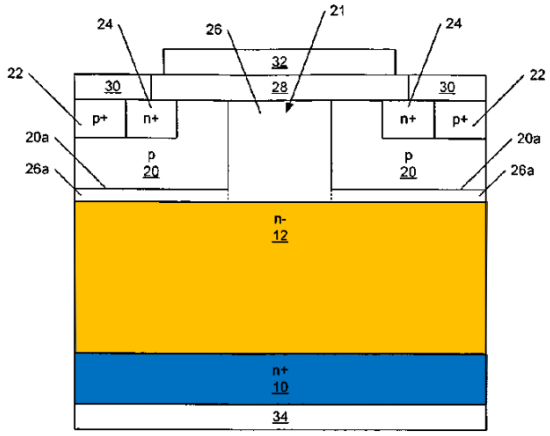
Ryu discloses that "the n+ **layer [10]** has a carrier concentration of from about 10^{18} to about 10^{21} cm^{-3}." EX1003, ¶40. Thus, *Ryu*'s **layer 10** has charged carriers or dopants of n-type (*i.e.*, "*first type impurities*") at a concentration of from about 10^{18} to about 10^{21} cm^{-3} (*i.e.*, "*first concentration*"). EX1035, ¶80.

***Ryu* structure**	**Concentration (cm^{-3})**	**EX1003 cite**
Layer 10	About 10^{18} to about 10^{21} ("*first concentration*")	¶40

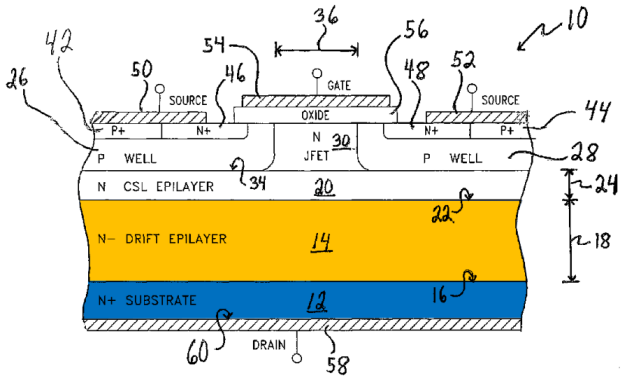
Therefore, *Ryu* discloses element 1[a]. EX1035, ¶81.

c) 1[b]: "a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;"

Ryu's Figure 2A (below, alongside the '633 patent's Figure 1), shows "a lightly doped n− **drift layer 12** of silicon carbide" (*i.e., "a drift semiconductor layer"*) on the n+ **layer 10**, just as drift layer 14 of the '633 patent is on its substrate 12. EX1003, ¶40. *Ryu* states that its **drift layer 12** is formed on substrate 10. *Id.*, ¶53 ("Alternatively, the drift layer 12 may be ***provided on an n+ silicon carbide substrate***."). EX1035, ¶82.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

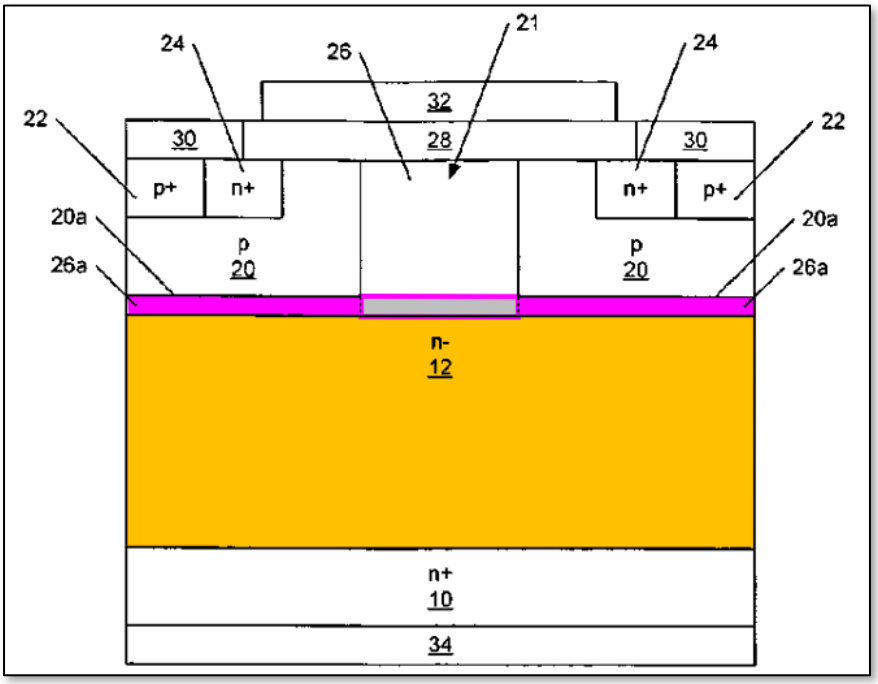
Ryu discloses that "the n− **drift layer 12** has a carrier concentration of from about 10^{14} to about 5×10^{16} cm^{-3}." EX1003, ¶40. Thus, *Ryu*'s **drift layer 12** has charged carriers or dopants of n-type (*i.e.*, "*first type impurities*") at a concentration from about 10^{14} to about 5×10^{16} cm^{-3} (*i.e.*, "*second concentration*"), which is less than the about 10^{18} to about 10^{21} cm^{-3} concentration (*i.e.*, "*the first concentration*") of **layer 10**. EX1035, ¶83.

***Ryu* structure**	**Concentration (cm^{-3})**	**EX1003 cite**
Layer 10	About 10^{18} to about 10^{21} ("*first concentration*")	¶40
Drift layer 12	About 10^{14} to about 5×10^{16} ("*second concentration*")	¶40

Therefore, *Ryu* discloses element 1[b]. EX1035, ¶84.

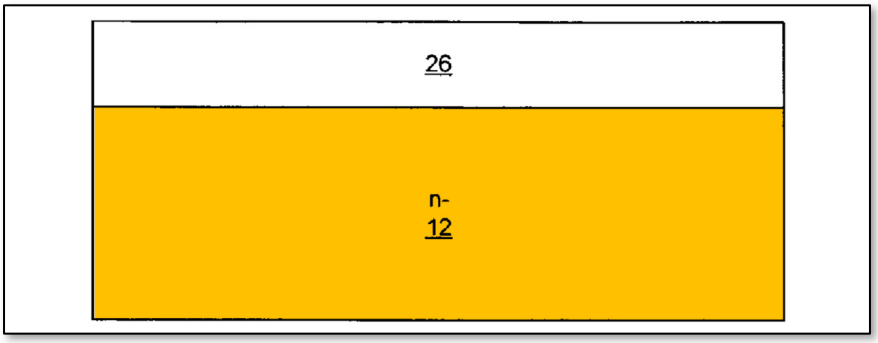
d) 1[c]: "a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;"

Ryu renders element 1[c] obvious. As shown in *Ryu*'s Figure 2A below, on top of the **drift layer 12** (*i.e.*, "*the drift semiconductor layer*"), are **regions 26a** colored magenta and a **strip** colored grey and outlined in magenta, between **regions 26a** and beneath region 21. As explained below, the **regions 26a** and the **strip** are "*a current spreading semiconductor layer formed on a front side of the drift semiconductor layer*." A POSITA would have understood *Ryu*'s **regions 26a** and the **strip** to be a "current spreading layer" both because, as explained below, current spreads laterally within it and *Ryu* forms that layer in the same way as the '633 patent forms its current spreading layer. EX1035, ¶85.



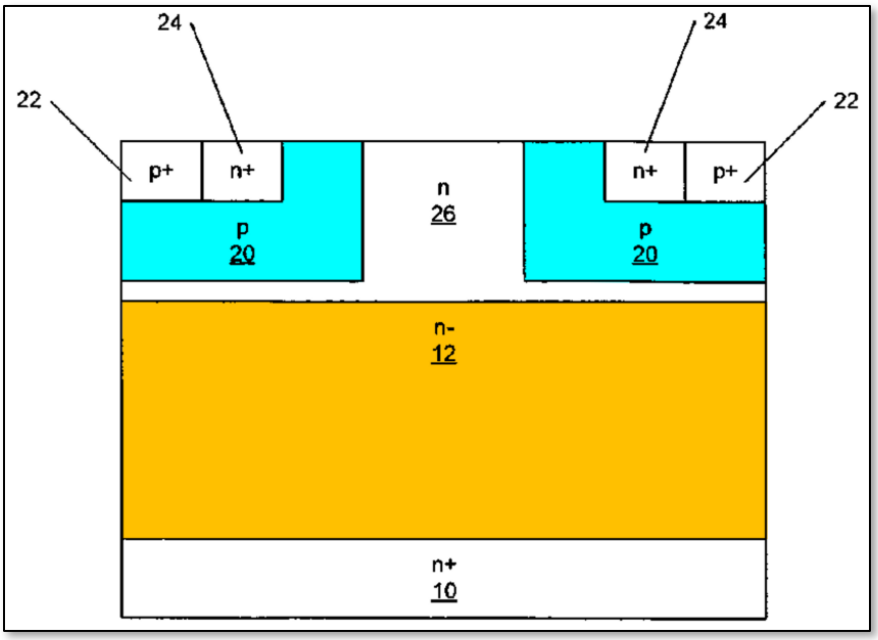
EX1003, FIG. 2A (annotated)

Ryu explains how its MOSFET in Figure 2A is formed: First, *Ryu* discloses that "[a] region of higher carrier concentration n-type silicon carbide 26 is provided on the **drift layer 12**." *Id.*, ¶41; *see also id.*, ¶53. At this fabrication stage, the structure looks as depicted in *Ryu*'s Figure 4A below. EX1035, ¶86.



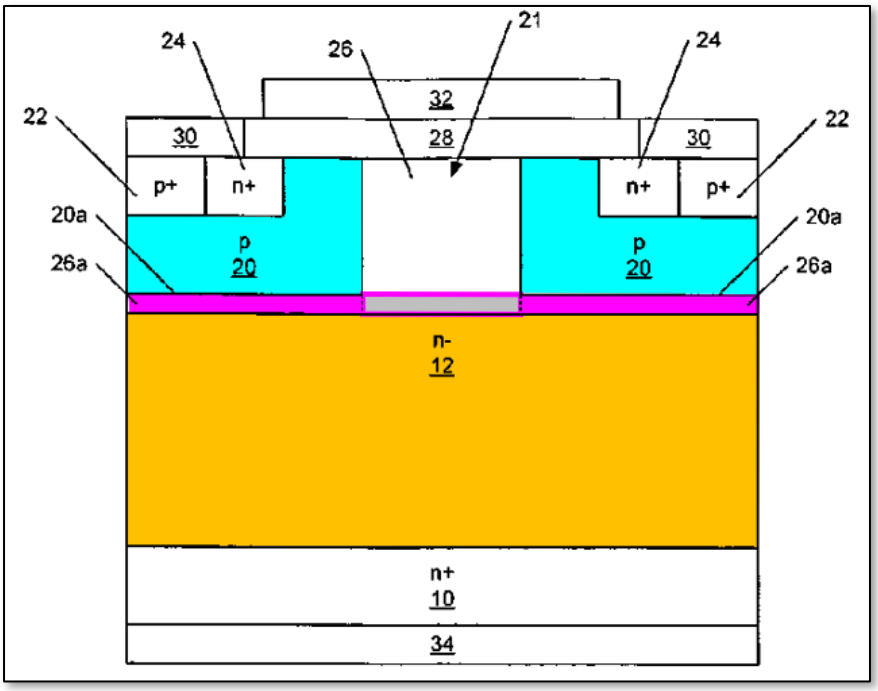
EX1003, FIG. 4A (annotated)

Next, *Ryu* teaches implantation steps forming **p-wells 20** (cyan below) and regions 22 and 24 within the p-wells 20, resulting in the Figure 4B structure below. *Id.*, ¶¶53–56. EX1035, ¶87.



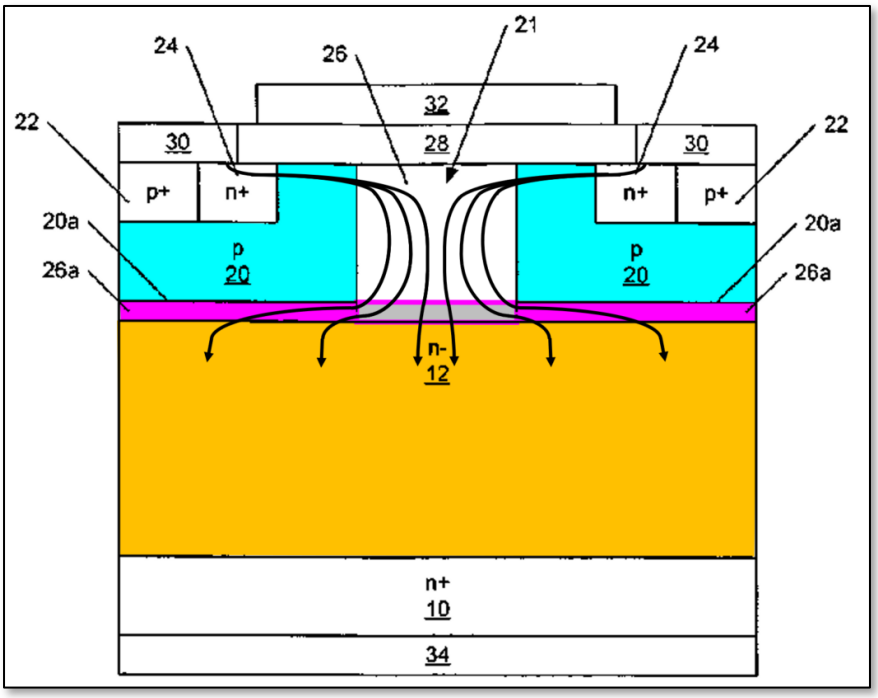
EX1003, FIG. 4B (annotated)

Region 21, **regions 26a**, and the **strip** (grey outlined in magenta below) all have the same doping concentration: they are the regions that remain from the original thick layer 26 (shown in Figure 4A above) and were unaffected by *Ryu*'s subsequent implantation steps. EX1035, ¶88.



EX1003, FIG. 2A (annotated)

As explained in Section X.A.1.g, *Ryu* explicitly discloses the gap 21 (identified by the arrow in Figure 2A) between the p-wells 20 as the JFET region 21. EX1003, ¶¶42, 44. Also, the **regions 26a** and the **strip** form a current spreading layer because, as current flows from the source downward through JFET region 21 towards the drain, the current experiences increased lateral flow in that layer before flowing down into the **drift layer 12** as depicted by the arrows in the figure below. The current "spreads" laterally in that layer. EX1035, ¶89.



EX1003, FIG. 2A (annotated)

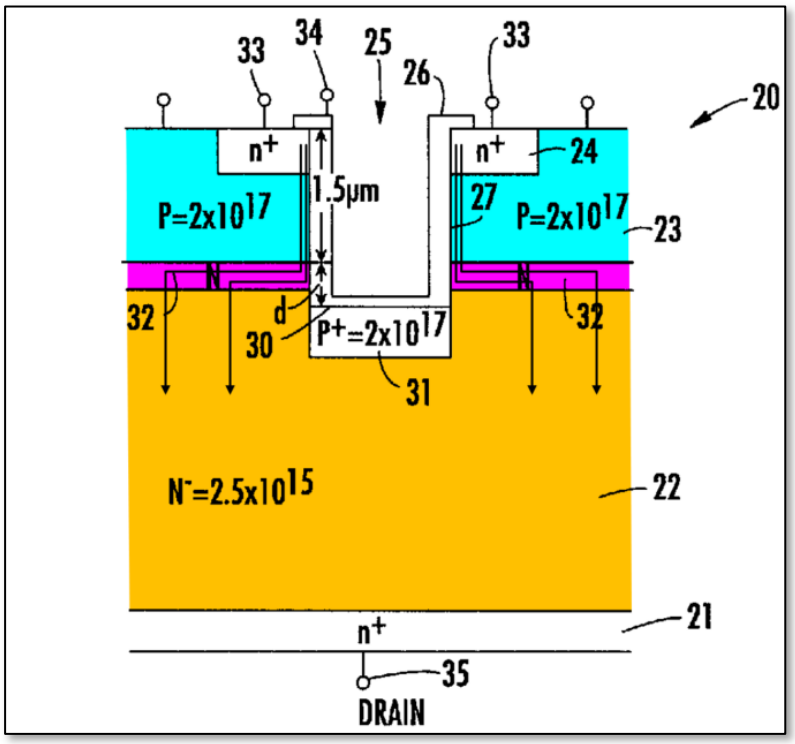
.It was known in the art that a JFET region is formed between two adjacent p-wells. *See, e.g.*, EX1033, H4.5.2 ("the JFET region formed by two adjacent p-well regions"); EX1029, FIG. 1, ¶2 ("The area between body regions 110a and 110b under gate 114 is commonly referred to as the JFET region."). Moreover, a POSITA would have understood that current flowing downward, underneath the JFET region and towards the drain, experiences increased lateral flow in the strip as depicted in the figure above. Thus, the JFET region 21 (*i.e.*, the gap 21 between the p-wells 20) overlies the strip, and a region exists in that strip beneath the floor of the p-wells 20 and above the drift layer 12 in which the current experiences increased lateral

flow.[5] Because of this, the **strip** together with the **regions 26a** forms a current spreading layer. EX1035, ¶90.

The reason the current spreads laterally in the layer formed by the **regions 26a** and the **strip** is that the electrical resistance of that layer is lower than the resistance of the **drift layer 12**. Because *Ryu* discloses that layer 26 is "of higher carrier concentration" than the **drift layer 12**, a POSITA would have understood that region 26, including **regions 26a** and the **strip**, is of lower resistance than the **drift layer 12**. EX1003, ¶41; *see, e.g.*, EX1032, 30, Figure 2.18 (illustrating resistivity decreasing as doping concentration increases); EX1019, 69 ("the epitaxial layer is more lightly doped and so has a higher resistivity"). Thus, a POSITA would have also understood that current flowing from the source through channels in the **p-wells 20** and down the JFET region 21 would spread laterally in the **strip** and **regions 26a** before flowing down into the higher resistance **drift layer 12**. For instance, in U.S. Patent No. 6,570,185 ("*Tan*1"), which was filed in 1997, a UMOSFET 20 illustrated in Figure 2 (below) includes a **current enhancing layer 32** with higher carrier

[5] Although *Ryu*'s Figure 2A depicts undescribed dotted lines between each **region 26a** and the **strip**, a POSITA would appreciate that there are no boundaries or practical differences—in structure, material, or otherwise—between **regions 26a** and the **strip**. EX1035, ¶90.

concentration over an **epitaxial layer 22**. EX1030, 4:20–25; 5:12–16. *Tan*1 teaches that, by adding the n-type **current enhancing layer 32**, "the current can first flow laterally inside the n-type layer, and then flow down to the drain." *Id.*, 4:47–49; *cf.* EX1001, 6:31–37 ("Because the doping concentration of the **current spreading layer 20** is greater than the doping concentration of the underlying **drift layer 14**, current tends to flow downwardly from the JFET region 30 and laterally through the **current spreading layer 20** before subsequently flowing down through the upper portion of the lower doped **drift layer 14**."). The lateral current flow in *Tan*1's **current enhancing layer 32** is depicted by the arrows in the figure below. EX1035, ¶91.



EX1030, FIG. 2 (annotated)

Similarly, in 1998 IEEE article titled "High-Voltage Accumulation-Layer UMOSFET's in 4H-SiC" ("*Tan*2"), listing the '633 patent's inventor Cooper as co-author, *Tan*2 discloses "an **n-type epilayer** under the **p-base** to promote lateral current spreading into the **drift region**." EX1031, Abstract. *Tan*2 illustrates, in Figure 1 (below), the lateral current flow in the **n-type epilayer**, depicted by the yellow arrows. The caption of *Tan*2's Figure 1 refers to the n-type epilayer as "an n-type ***current-spreading epilayer***." *Tan*2 explains "[t]he doping of this n-type epilayer is about 100x higher than that of the n-drift region." *Id.*, 488. A POSITA would have understood *Ryu*'s **regions 26a** and **strip** to function like *Tan*1's **current enhancing layer 32** and *Tan*2's **current-spreading epilayer**. EX1035, ¶92.

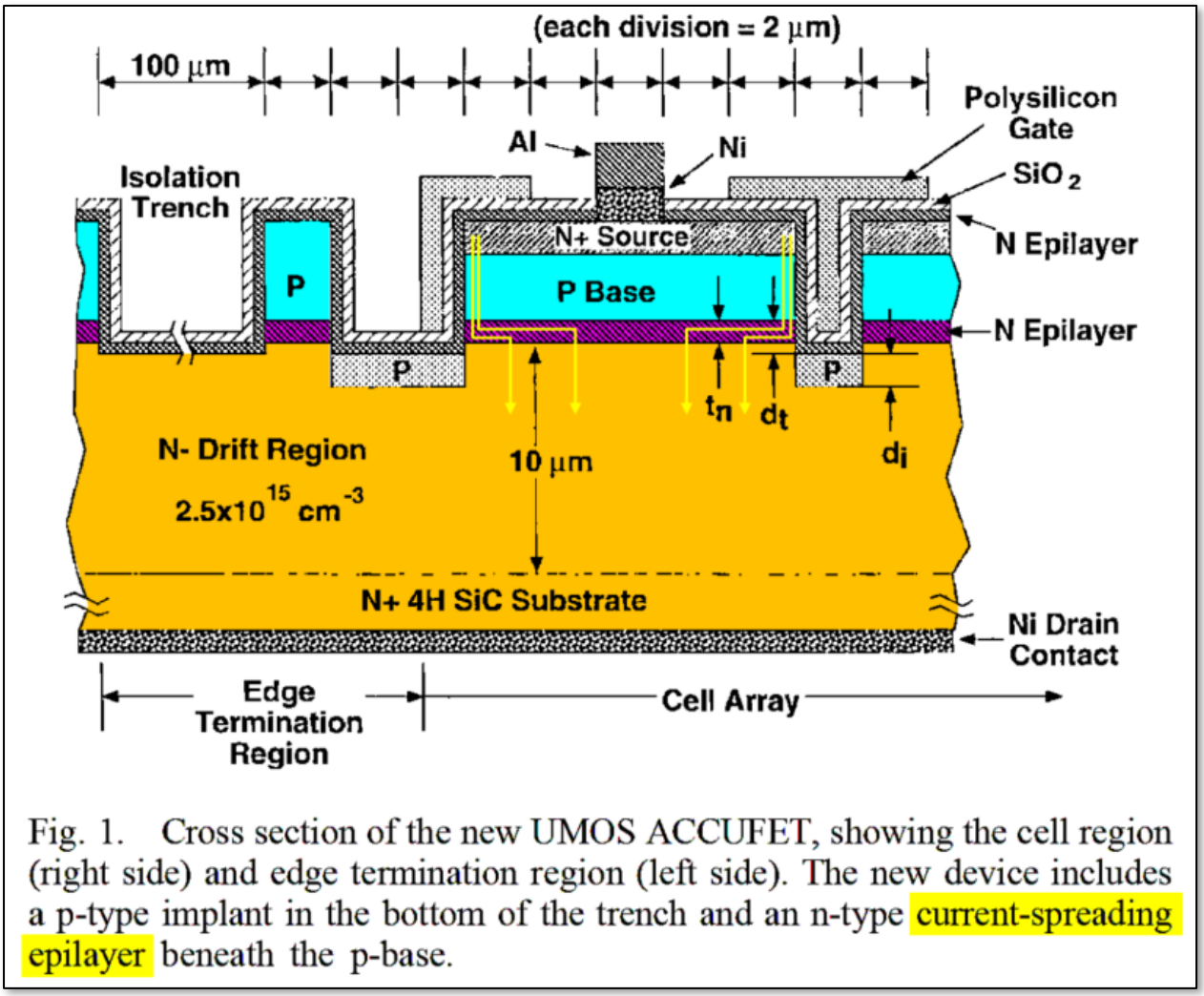


Fig. 1. Cross section of the new UMOS ACCUFET, showing the cell region (right side) and edge termination region (left side). The new device includes a p-type implant in the bottom of the trench and an n-type current-spreading epilayer beneath the p-base.

EX1031, Figure 1 (annotated)

Ryu forms **regions 26a**, and the **strip**, using fabrication processes like those the '633 patent uses to form the **CSL 20**. *Ryu* discloses that "[a] region of higher carrier concentration n-type silicon carbide 26 is provided on the **drift layer 12**" and "[t]he **p-wells 20** are implanted." EX1003, ¶¶41–42. Similarly, the '633 patent describes "growing an extra-thick current spreading layer 20 and forming the **'P'**

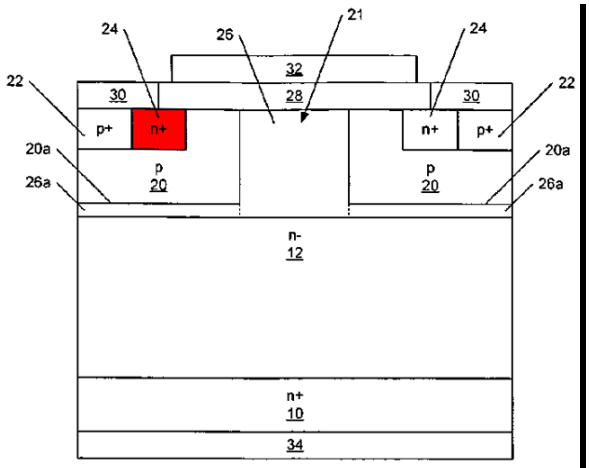
wells 26, 28 using a suitable incorporation process such as an ion implantation process." EX1001, 5:57–60. EX1035, ¶93.

Thus, *Ryu*'s **regions 26a** and the **strip**, together, are "*a current spreading semiconductor layer formed on a front side of the drift semiconductor layer*." *Id.*, ¶94.

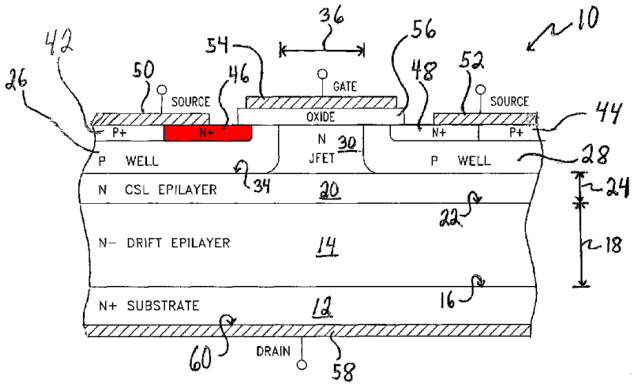
e) 1[d]: "a first source region;"

Ryu discloses element 1[d]. *Ryu* discloses that "**regions of n+ silicon carbide 24** . . . are disposed within p-wells 20." EX1003, ¶45. A POSITA would have understood *Ryu*'s **n+ regions 24** to be source regions because they: (1) are contacted by source contacts 30; and (2) correspond to the same "source regions" both in *Ryu* and Ryu's other articles describing the same structure. EX1035, ¶95.

First, *Ryu* explains that "***source*** contacts 30 . . . provide ohmic contact to . . . the **n+ regions 24**." EX1003, ¶47; *see also id.*, claims 6 and 36 ("a source contact on the first n-type silicon carbide region"). A POSITA would have understood that the **n+ regions 24** are ***source*** regions because they are contacted by the ***source*** contacts 30. Likewise, the '633 patent forms "source metallic electrode 50, 52 … over the source regions 46, 48, respectively" to achieve the same function. EX1001, 7:4-6. A comparison of *Ryu*'s Figure 2A and the '633 patent's Figure 1 also shows that *Ryu*'s **n+ regions 24** correspond to the '633 patent's **source regions 46 and 48** and are similarly of n-type doping at an "n+" concentration. EX1035, ¶96.

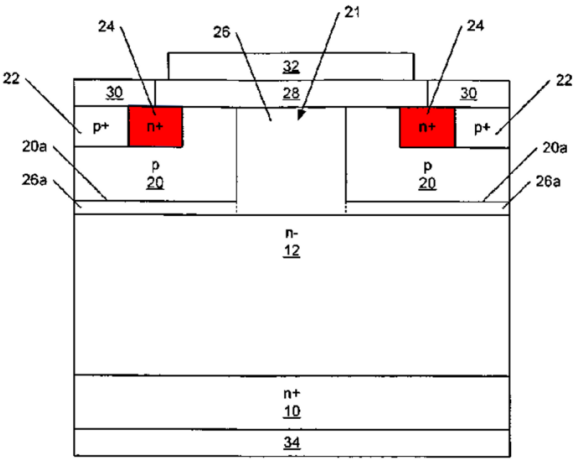


EX1003, FIG. 2A (annotated)

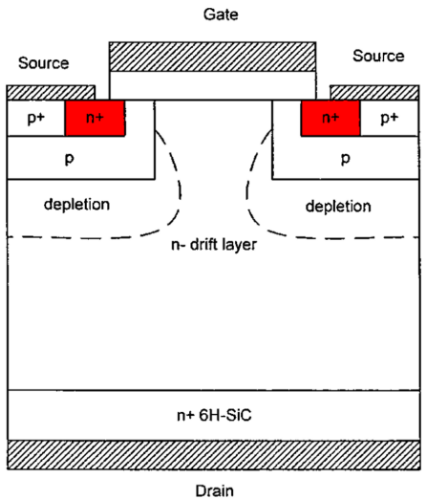


EX1001, FIG. 1 (annotated)

Second, the **n+ regions 24** in *Ryu*'s Figure 2A correspond, in location and relative position to other structures, to the n+ regions in *Ryu*'s conventional double-implanted MOSFET of Figure 1. EX1003, ¶27. *Ryu*'s Figures 1 and 2A are below with the n+ regions in red. *Ryu* explicitly discloses that the n+ regions in Figure 1 are "source regions." *Id.*, ¶6 ("***source regions (n+)***"). A POSITA would have understood that the **n+ regions 24** in Figure 2A correspond to the **n+ regions** in *Ryu*'s Figure 1 and are all source regions. EX1035, ¶97.

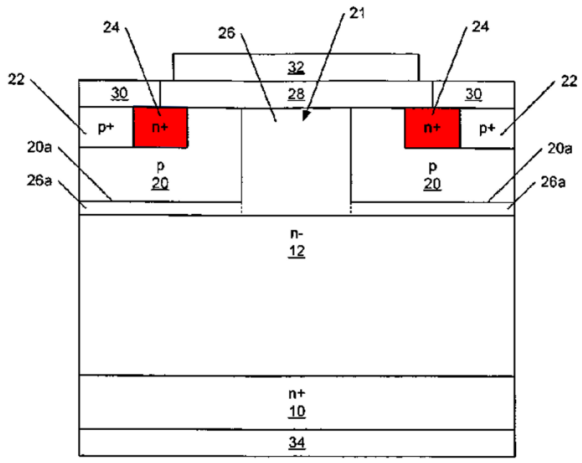


EX1003, FIG. 2A (annotated)

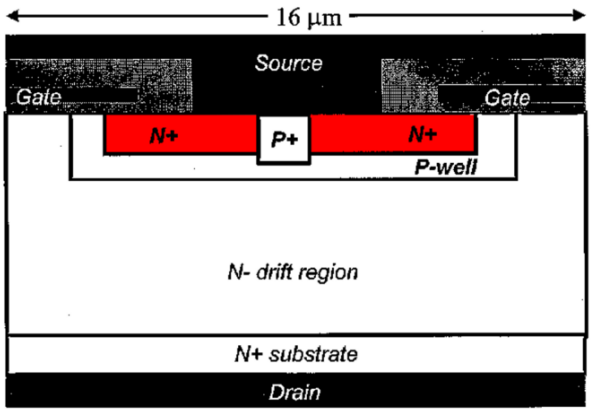


EX1003, FIG. 1 (annotated)

The **n+ regions 24** in *Ryu*'s Figure 2A correspond to the N+ regions in the "DiMOSFET" in Ryu's Figure 1 (below, with the N+ regions in red) of a 2002 article titled "10 A, 2.4 kV Power DiMOSFETs in 4H-SiC." EX1023, Figure 1; *see also* EX1024, Figure 2. EX1035, ¶98.



EX1003, FIG. 2A (annotated)



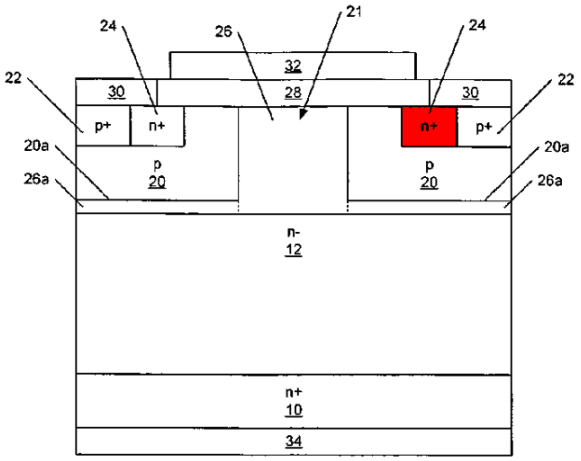
EX1023, FIG. 1 (annotated)

Ryu's articles explicitly disclose that the N+ regions are "source regions." EX1024, 881 ("n+ source regions were formed by nitrogen implantation"); *see also* EX1023, 321 ("***N+ source regions***"). Accordingly, a POSITA would have understood *Ryu*'s **n+ regions 24** in Figure 2A to be ***source*** regions. EX1035, ¶¶99–100.

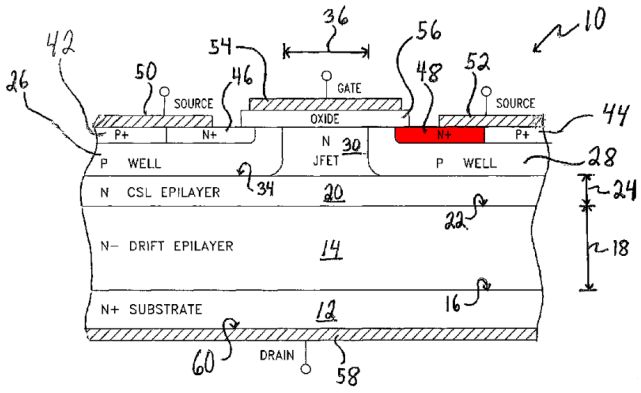
Thus, for example, *Ryu* discloses at least a first **n+ region 24** (*i.e.*, "*a first source region*") on the left in Figure 2A. *Id.*, ¶101.

f) 1[e]: "a second source region;"

Ryu discloses element 1[e]. As discussed above for element 1[d], *Ryu*'s **n+ regions 24** are source regions and correspond to the '633 patent's **source regions 46 and 48**. Thus, *Ryu* discloses at least a second **n+ region 24** (*i.e.*, "*a second source region*") on the right as shown below. EX1035, ¶102.



EX1003, FIG. 2A (annotated)



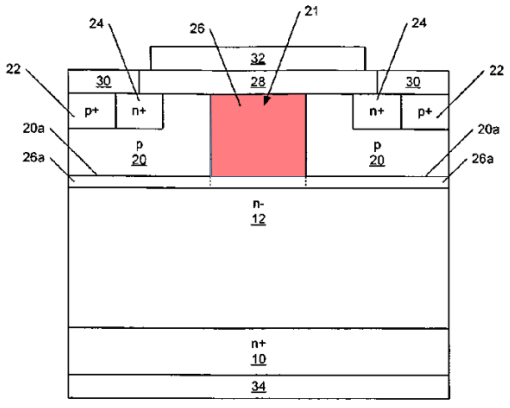
EX1001, FIG. 1 (annotated)

g) 1[f]: "a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities;"

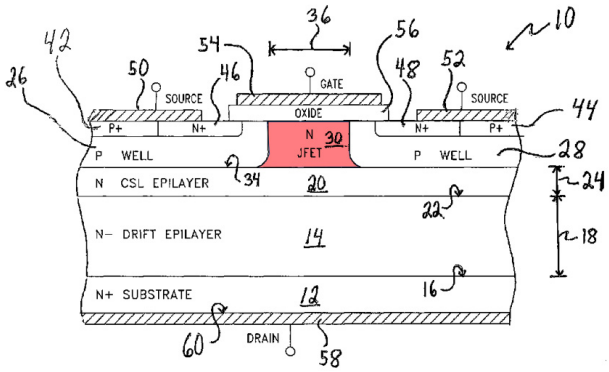
Ryu discloses element 1[f]. *Ryu* expressly discloses a "*JFET region*" formed on a front side of the **regions 26a** and the **strip** (*i.e.*, together "*the current spreading layer*") and defined between the left and right **n+ regions 24** (*i.e.*, "*the first source region and the second source region*") just as in the '633 patent. *Ryu*'s JFET region is of a higher concentration than its **drift layer 12**. EX1035, ¶103.

i. "a JFET region"

Ryu expressly discloses that the gap 21 (identified by the arrow in Figure 2A) between the p-wells 20 "may be referred to as the **JFET region 21**." EX1003, ¶¶42, 44; *cf.* EX1001, 5:57–59 ("the JFET region 30 may be formed by growing an extra-thick current spreading layer 20 and forming the "P" wells 26, 28"); *id.*, 6:3–5 ("The remaining region of the additional epitaxial layer between the wells 26, 28 forms the JFET region 30."); EX1033, H4.5.2 ("the JFET region formed by two adjacent p-well regions"); EX1029, FIG. 1, ¶2 ("The area between body regions 110a and 110b under gate 114 is commonly referred to as the JFET region."). *Ryu*'s **JFET region 21** in Figure 2A is shown beside the '633 patent's **JFET region 30** below, both in salmon. EX1035, ¶104.



EX1003, FIG. 2A (annotated)

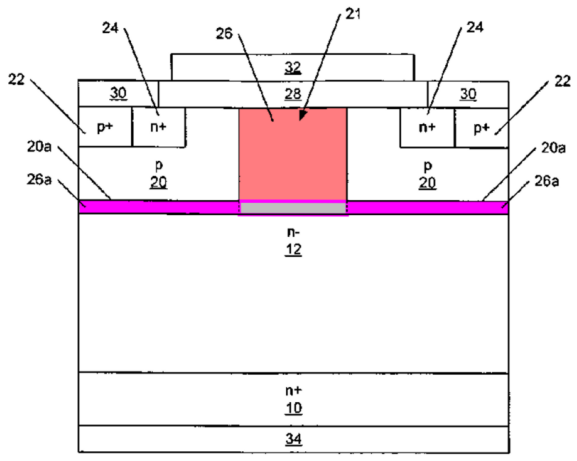


EX1001, FIG. 1 (annotated)

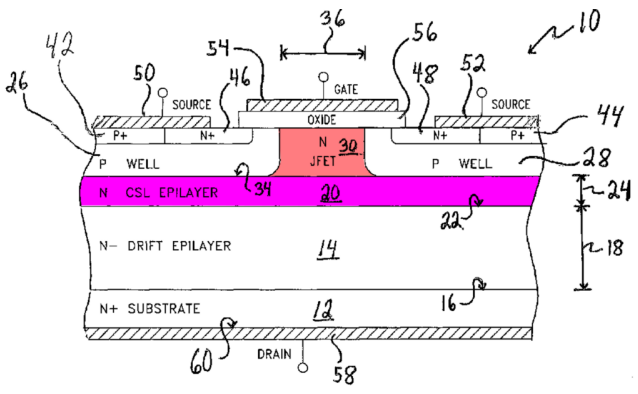
ii. "formed on a front side of the current spreading semiconductor layer"

As discussed above, *Ryu* discloses the **JFET region 21** as the gap 21 between the p-wells 20. EX1003, ¶¶42, 44. A POSITA would have understood that *Ryu*'s

JFET region 21 is located between the p-wells 20 and not past their floors 20a, such that the strip between regions 26a is not part of the JFET region 21. *See, e.g.*, EX1033, H4.5.2 ("the JFET region formed by two adjacent p-well regions"); EX1029, FIG. 1, ¶2 ("The area between body regions 110a and 110b under gate 114 is commonly referred to as the JFET region."). As discussed above with respect to element 1[c], *Ryu*'s regions 26a and the strip, together, correspond to "*the current spreading layer*." As shown in *Ryu*'s Figure 2A, below alongside the '633 patent's Figure 1, *Ryu*'s JFET region 21 corresponds to the '633 patent's JFET region 30 and is formed on the front side of *Ryu*'s regions 26a and the strip (*i.e.*, "*the current spreading layer*"), just like the '633 patent's JFET region 30 is formed on the front side of the CSL 20. EX1035, ¶105.



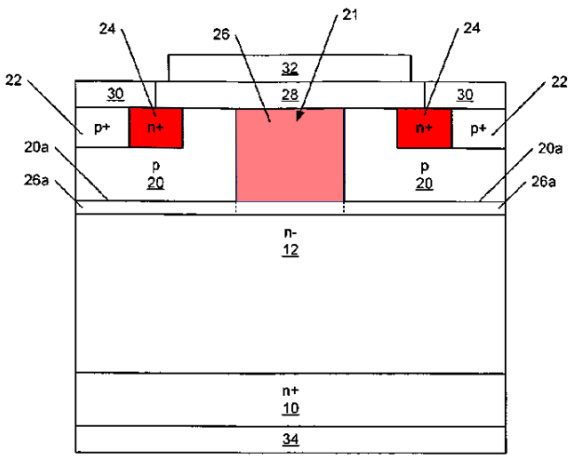
EX1003, FIG. 2A (annotated)



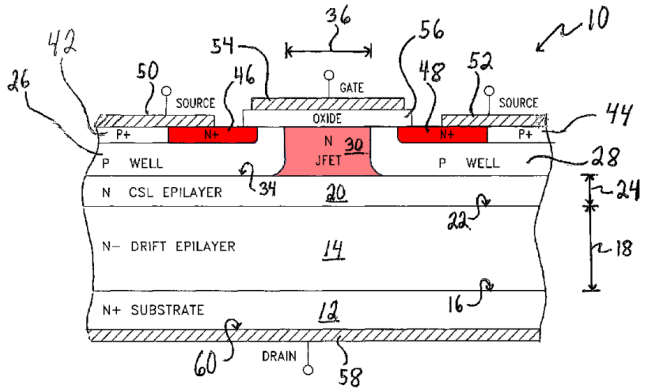
EX1001, FIG. 1 (annotated)

iii. "defined between the first source region and the second source region"

Ryu discloses the "gap between the p-wells 20 (the region which may be referred to as the **JFET region 21**)." EX1003, ¶44; *see also id.*, ¶42 ("the gap 21 between the p-wells 20"). As depicted in *Ryu*'s Figure 2A, the **JFET region 21** is between the p-wells 20 and between *Ryu*'s **n+ regions 24** (*i.e.*, "*the first source region and the second source region*"), which are themselves disposed within p-wells 20. As shown below, *Ryu*'s arrangement is identical to that of the '633 patent, where both structures include a portion of each p-well between the source regions and the JFET region. Accordingly, *Ryu*'s **JFET region 21** is "*defined between the first source region and the second source region*" just like the '633 patent's JFET region. EX1035, ¶106.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

iv. "the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities"

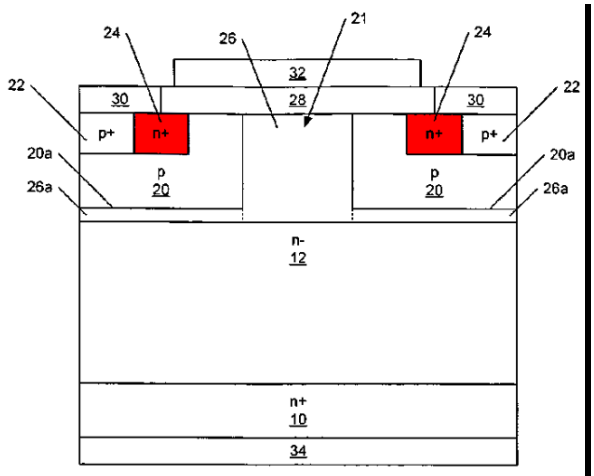
Ryu discloses that "the gap 21 [(*i.e.*, the **JFET region 21**)] between the p-wells 20 has a higher carrier concentration than the **drift layer 12**." EX1003, ¶42. Indeed, because the **JFET region 21** is formed in region 26, it has the region 26's n-type (*i.e.*, "*first type impurities*") carrier concentration of "from about 10^{15} to about 5×10^{17} cm^{-3}" (*i.e.*, "*a third concentration*"), which is greater than the carrier concentration of from about 10^{14} to about 5×10^{16} cm^{-3} (*i.e.*, "*the second concentration*") of the **drift layer 12**. *Id.*, ¶¶40–41; EX1035, ¶107.

***Ryu* structure**	**Concentration (cm^{-3})**	**EX1003 cite**
Layer 10	About 10^{18} to about 10^{21} ("*first concentration*")	¶40
Drift layer 12	About 10^{14} to about 5×10^{16} ("*second concentration*")	¶40
JFET region 21	About 10^{15} to about 5×10^{17} ("*third concentration*")	¶41

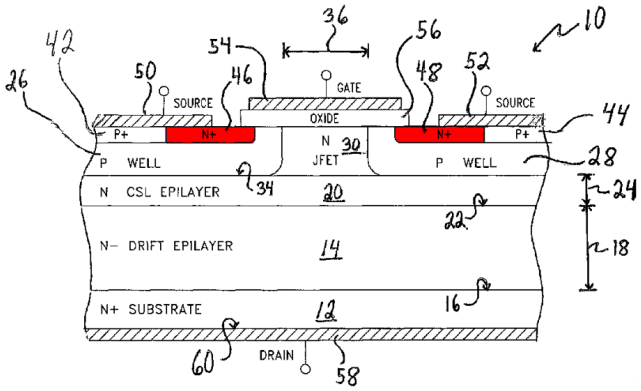
h) 1[g]: "a plurality of source regions; and"

The combination of *Ryu* and *Williams* renders element 1[g] obvious. As discussed above with respect to elements 1[d] and 1[e], *Ryu* discloses at least a left

n+ region 24 (*i.e.*, *a first source region*) and a right **n+ region 24** (*i.e.*, *a second source region*). EX1035, ¶108.



EX1003, FIG. 2A (annotated)

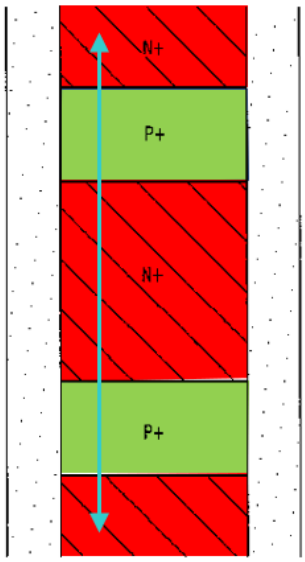


EX1001, FIG. 1 (annotated)

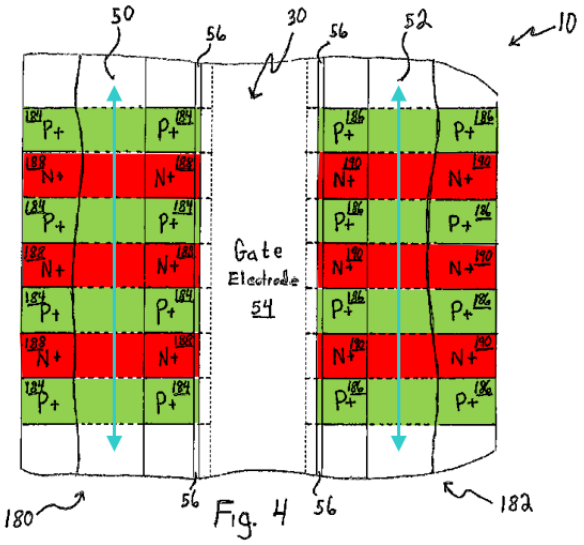
Ryu does not explicitly disclose a plurality of source regions in addition to the left and right **n+ regions 24**, showing the **n+ regions 24** only in cross-section, and not from a top view. But *Williams* does show a top view of such source regions and, as explained below, it would have been obvious to use *Williams*'s source regions structure in *Ryu*. EX1035, ¶109.

Williams discloses vertical MOSFETs having linear cellular configurations. EX1004, Figures 4A, 7A–7B, and 18. *Williams* explains that "[t]he source and body contact construction can also be varied geometrically . . . as shown in the plan views of FIGS. 19A–19F." *Id.*, 16:28-30. *Williams* discloses a "'bamboo' ladder structure (alternating **N+** and **P+** regions)" in the plan view of Figure 19D (below), where a plurality of **N+ source regions** are linearly spaced from each other, alternatingly

with **P+ body contact regions**, in a direction indicated by the teal arrow, just as shown in the '633 patent's Figure 4. EX1004, 10:21–22. EX1035, ¶110.



EX1004, FIG. 19D (annotated)



EX1001, FIG. 4 (annotated)

The obviousness of using *Williams*'s linear **N+ source regions** configuration in *Ryu* is further shown by many other references, as discussed herein, which demonstrate that MOSFETs with linear geometry were notoriously well-known. *See, e.g.*, EX1019, 455 ("one manufacturer advocates the use of a linear metal gate structure"); EX1018, 238 ("A typical example of linear placement is the placement of a linear array"); *see also* EX1017, 186. EX1035, ¶¶111–113.

Accordingly, a POSITA would have been motivated to use a linear geometry and found it obvious to construct *Ryu*'s MOSFET in view of *Williams*'s teachings of a linear cellular structure and bamboo/ladder source-body structure of Figure 19D such that *Ryu*'s cross-sectional view of its MOSFET would extend in a direction

perpendicularly to the page and *Ryu*'s left and right **n+ regions 24** and **p+ regions 22** (which, as explained in Section X.A.1.i, are base/body contact regions) would be replicated alternatingly in the same direction. EX1035, ¶114.

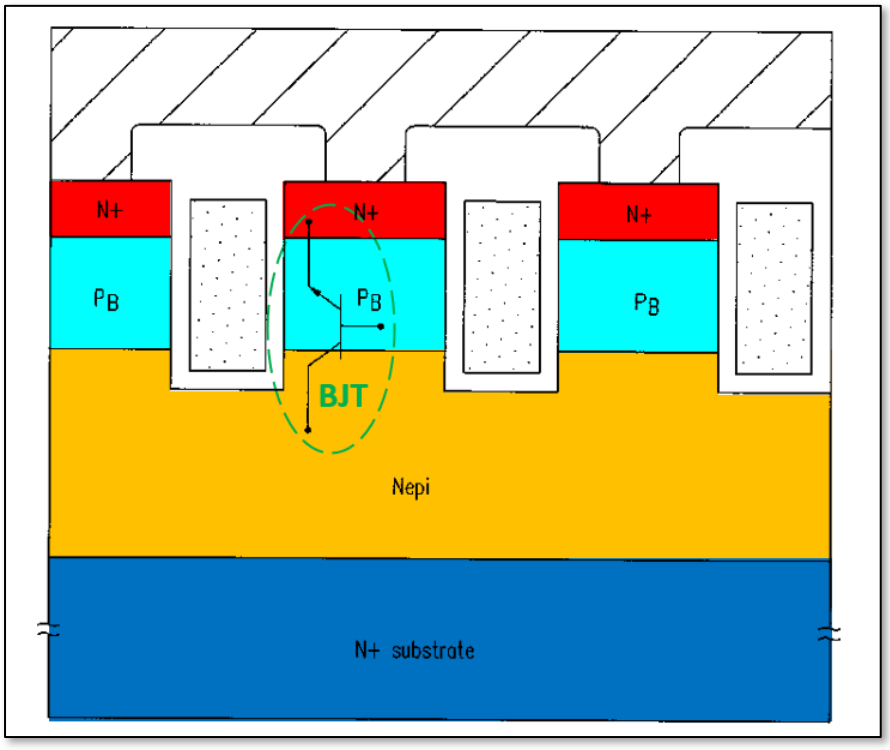
i. Motivation to Combine Ryu and Williams

A POSITA would have been motivated to implement *Ryu*'s MOSFET according to *Williams*'s teachings such that *Ryu*'s MOSFET is formed using a linear cell structure having a plurality of left and right **n+ regions 24** and **p+ regions 22** replicated alternatingly in a direction perpendicularly to the page. EX1035, ¶115.

Ryu and *Williams* are from the same field of endeavor. *See, e.g.*, *Medtronic, Inc. v. Cardiac Pacemakers, Inc.*, 721 F.2d 1563, 1574–75 (Fed. Cir. 1983); M.P.E.P. § 2141. Both references are directed to vertical MOSFETs. *Ryu* discloses embodiments of vertical MOSFETs that "may reduce on-state resistance" compared to conventional vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1. *Williams* discloses structures for vertical MOSFETs that are used to reduce on-resistance. *See, e.g.*, EX1004, , Figure 1, 8:15–16 ("reduce the on-resistance of the DMOSFET"), 16:31–32 ("achieve the lowest possible resistance"). Thus, both references are directed to vertical MOSFETs and aim at reducing on-resistance. EX1003, ¶6; EX1004, 1:7–8. EX1035, ¶116.

Although *Williams* discloses MOSFETs with a so-called trench gate and *Ryu* discloses a MOSFET with a so-called planar gate, a POSITA would nonetheless

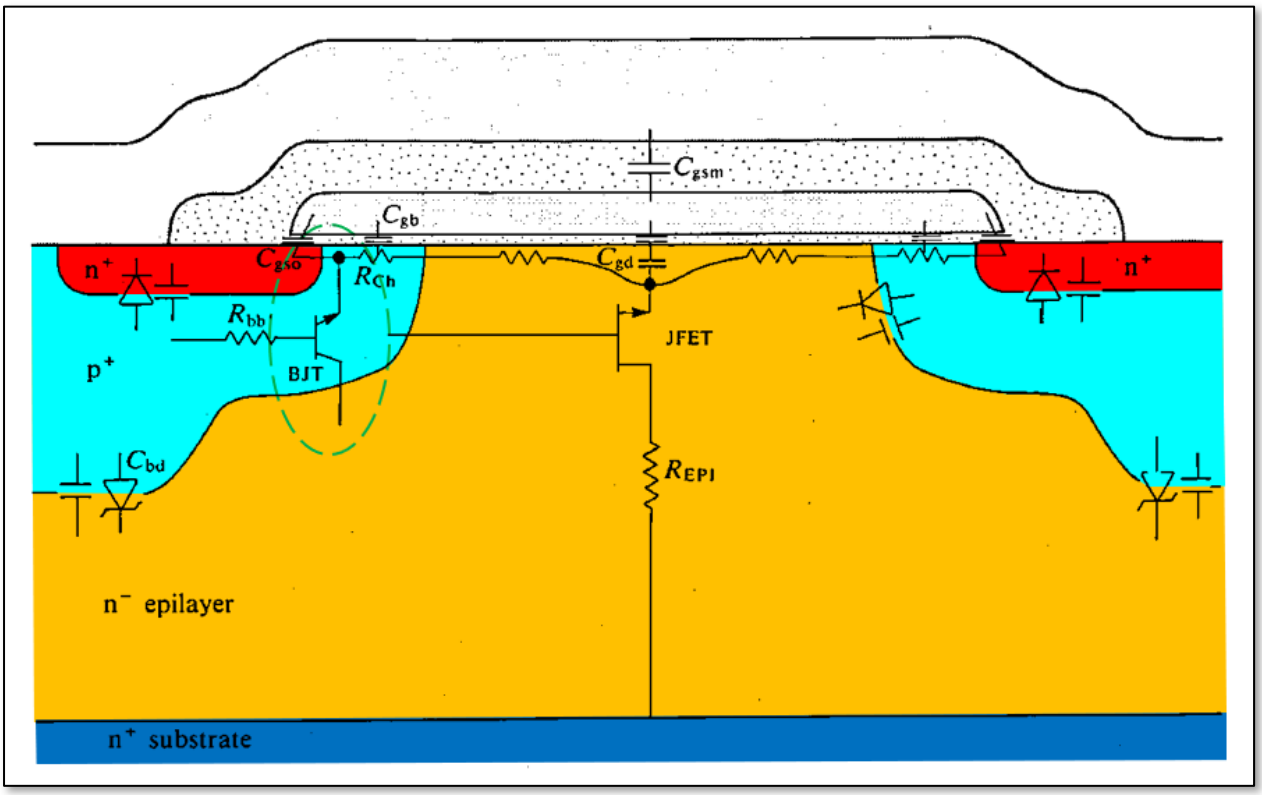
have been motivated to use *Williams*'s teachings in *Ryu*. This is because *Williams*'s and *Ryu*'s MOSFETs share many common features to which the shape of the gate is irrelevant. For example, both *Williams*'s trench-gated vertical MOSFETs and *Ryu*'s non-trench-gated vertical MOSFET include a parasitic BJT within the epilayer that could inadvertently be activated. For both *Williams* and *Ryu*, the solution to the potential problem caused by this parasitic transistor is the same. For example, *Williams* describes such a "parasitic NPN bipolar transistor," which it illustrates in Figure 7A (below). EX1004, 6:9. EX1035, ¶117.



EX1004, FIG. 7A (annotated)

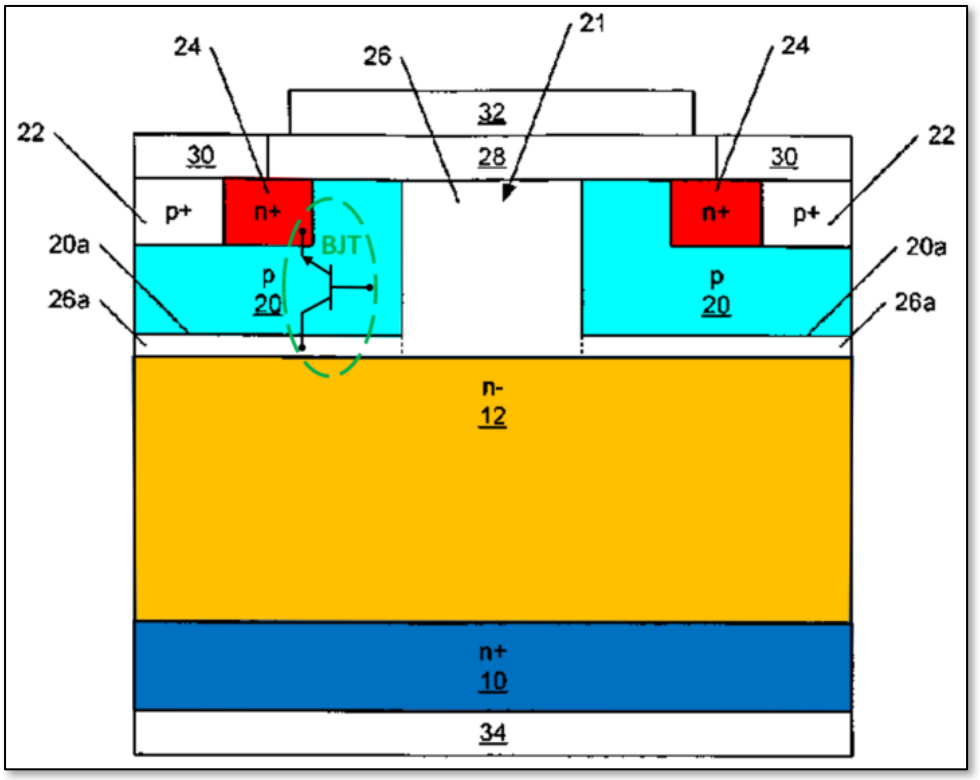
Williams's parasitic BJT is formed between the source, the body, and the drain like *Grant* illustrates a parasitic "npn bipolar junction transistor (BJT) formed

between the source, the body, and the drain" of a non-trench-gated vertical MOSFET in Figure 3.15, reproduced below. EX1019, 81. EX1035, ¶118.



EX1019, Figure 3.15 (annotated)

Based on at least *Grant*'s teachings, a POSITA would have understood that a parasitic npn BJT would also be formed in *Ryu*'s MOSFET between the n+ region 24 (*i.e.*, source region), p-well 20 (*i.e.*, body), and the n-type epitaxial layer 26 (*i.e.*, portion of drain region), as annotated in *Ryu*'s Figure 2A below. *See* EX1003, ¶53. EX1035, ¶119.



EX1003, FIG. 2A (annotated)

Both *Ryu* and *Williams* prevent the parasitic BJT from activating by shorting the source to the body, via p+ diffusion, using a source electrode. EX1003, Figure 2A (illustrating **source contacts 30** shorting **n+ regions 24** to p-wells 20 via **p+ regions 22**); *see, e.g.*, EX1004, Figure 15D, 15:6–8 ("Metal layer [158] contacts both N+ source region 159 and P+ body contact region 160, thereby shorting the source and body together."). *See also* Section VI.D. At least because *Ryu* and *Williams* share the common problem preventing the parasitic BJT from activating, and solve that problem in the same way, *i.e.*, by shorting the body to the source, a

POSITA would have recognized that *Williams*'s well-known linear geometry was applicable in *Ryu*. EX1035, ¶120.

Furthermore, although *Ryu* is directed to silicon-carbide MOSFETS and *Williams* to silicon MOSFETs, *Baliga* teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." EX1005, 4:22–38. *Ghezzo* also teaches a method of replacing the conventional double-diffusion used in silicon MOSFETs with a double ion implantation sequence for SiC MOSFETs. EX1021, 1:56–63. EX1035, ¶121.

Accordingly, a POSITA would have understood that the teachings of *Williams* were directly applicable to *Ryu*'s SiC MOSFETs. *Id.*, ¶122.

Implementing *Ryu*'s MOSFET in a linear cell structure such that *Ryu*'s left and right **n+ regions 24** and **p+ regions 22** are replicated alternatingly in a direction perpendicular to the page as taught by *Williams* would have yielded expected, predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007); M.P.E.P. 2143(I)(A). *Ryu* discloses adjacent **n+ region 24** and **p+ region 22** disposed within the p-well 20 in a cross-sectional view of a MOSFET in Figure 2A. EX1003, ¶45. *Williams* also discloses adjacent N+ source region 12 and a P+ body contact region 13 in a cross-sectional view of a MOSFET in Figure 1. EX1004, 1:9–10. Additionally, *Williams* teaches, in a plan view in Figure 19D, alternating **N+**

source regions and **P+ body contact regions** in an up-down direction with respect to the page. A POSITA would have been motivated to combine the elements taught by *Ryu* and *Williams*—namely, the adjacent **n+ region 24** and **p+ region 22** as taught by *Ryu*, and the alternating **N+ source regions** and **P+ body contact regions** in an up-down direction with respect to the page as taught by *Williams*—using known and routine semiconductor fabrication techniques to modify the shapes and locations of *Ryu*'s **n+ regions 24** and **p+ regions 22** such that *Ryu*'s **n+ regions 24** and **p+ regions 22** are replicated alternatingly in a direction perpendicular to the page because, as *Williams* teaches, such a configuration "does not comprise N+ contact resistance at all." EX1004, 17:5–6. This result would have been readily predictable and recognized by a POSITA because, as *Williams* points out, in its bamboo or ladder structure of Figure 19D, "the N+ source is contacted along its length except for an occasional P+ strap." *Id.*, 17:7–8. A POSITA would have appreciated, from *Williams*'s teachings, that there are design choices to be made when designing and fabricating MOSFETs, including trade-offs between maximizing the area of the **N+ source regions** and maximizing the contact of the **P+ body contact regions** to the body region. *Id.*, 16:28-35 ("The design can be selected to maximize the N+ source perimeter (to achieve the lowest possible resistance) or to maximize the P+ contact to the body region (to suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device), or to compromise between the two."). The former reduces

on-resistance but makes the device less rugged, while the latter makes the device more rugged at the expense of higher on-resistance. To achieve the right balance between on-resistance and ruggedness, a POSITA would have been motivated to modify *Ryu*'s **n+ regions 24** and **p+ regions 22** according to *Williams*'s Figure 19D to not compromise the source contact resistance, while also maintaining the ruggedness of *Ryu*'s MOSFET by regularly shorting the **n+ regions 24** to the p-wells 20 via **p+ regions 22**. EX1035, ¶123.

A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because it would have been a simple substitution of one known element (adjacent **n+ region 24** and **p+ regions 22** in *Ryu*) for another (alternating **N+ source regions** and **P+ body contact regions** as taught by *Williams*) to obtain predictable results. *KSR*, 550 U.S., 416; M.P.E.P. 2143(I)(B). This substitution would have been readily achievable by a POSITA via known and routine semiconductor fabrication techniques to form *Ryu*'s **n+ regions 24** and **p+ regions** alternatingly in a direction perpendicularly to the page. EX1035, ¶124.

A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because forming *Ryu*'s **n+ regions 24** and **p+ regions 22** alternatingly in a direction perpendicular to the page according to *Williams*'s source-body design of Figure 19D would have been obvious to try. *KSR,* 550 U.S., 421; M.P.E.P. 2143(I)(E). As *Williams* illustrates in Figures 19A–19F, there were

numerous (at least six) known and predictable choices for forming adjacent **N+** and **P+** regions. A POSITA could have pursued these potential solutions with a reasonable expectation of success because the analysis would have simply involved trying each one of these solutions. *See, e.g., CRFD Research, Inc. v. Matal*, 876 F.3d 1330, 1347 (Fed. Cir. 2017) ("[A] person of ordinary skill would have two predictable choices … providing [the] person of ordinary skill with a simple design choice" of choosing one solution or the other). Thus, it would have been obvious to a POSITA to have formed *Ryu*'s **n+ regions 24** and **p+ regions 22** alternatingly in a direction perpendicular to the page, as *Williams* teaches in Figure 19D. EX1035, ¶125.

The modification of *Ryu*'s **n+ regions 24** and **p+ regions 22** to be in the form of *Williams*'s alternating **N+ source regions** and **P+ body contact regions** would have been readily implemented by simply modifying the masks used to form *Ryu*'s **n+ regions 24** and **p+ regions 22**. A POSITA could have implemented this modification using basic semiconductor fabrication techniques to modify *Ryu*'s masks such that *Ryu*'s **n+ regions 24** and **p+ regions 22** are formed alternatingly in a direction perpendicular to the page as taught by *Williams*. This modification would have been well within the knowledge and skillset of a POSITA. Indeed, the '633 patent implicitly confirms this. When the '633 patent discusses the different geometric shapes for the N+/P+ regions in Figures 2, 3 and 4, there is no discussion

of special manufacturing steps required, but only the advantages and disadvantages of the shapes themselves. EX1035, ¶126.

ii. Reasonable Expectation of Success in Combining Ryu and Williams

A POSITA would also have had a reasonable expectation of success. The combination of *Ryu* and *Williams* represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a POSITA would have been familiar with and been able to implement, and which *Williams* explains how to accomplish. EX1004, 26:38–27:32 ("Source/Mesa Formation") ; *id.*, 29:1–19 ("P+ Body Contact Formation"). The reasons a POSITA would have expected success parallel those that provide motivation for this combination—including because both *Ryu* and *Williams* are directed to vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1; EX1004, Abstract, 1:7–8, Figure 1. As discussed above, linear cell geometry was well known and a POSITA would have expected a linear cell implementation of *Ryu*'s structure to operate, just as linear cell implementations of other MOSFETs were known to operate. A POSITA would have had a reasonable expectation of success in implementing *Ryu*'s MOSFET in a linear geometry because *Ryu*'s underlying specification was designed to be extensible and flexible in its application to well-known cellular shapes and layouts. EX1003, ¶¶38 ("This invention may, however,

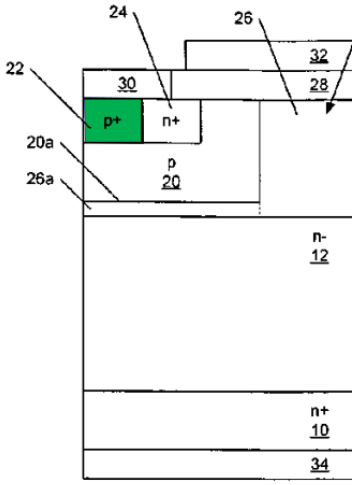
be embodied in many different forms…"), 63, 66. Such modifications were expected to be performed when optimizing the on-resistance and ruggedness of power MOSFETs. *See, e.g.*, EX1004, 16:28–17:19. EX1035, ¶127.

Accordingly, *Ryu* in view of *Williams* renders obvious element 1[g] and a POSITA would have been motivated to combine the teachings of these references and would have had a reasonable expectation of success. *Id.*, ¶128.

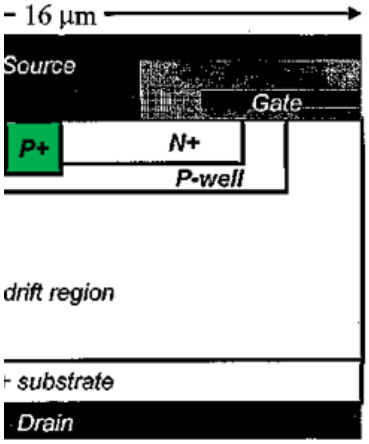
i) 1[h]: "a plurality of base contact regions,"

Ryu discloses that "**regions of p+ silicon carbide 22** are disposed within p-wells 20." EX1003, ¶45. A POSITA would have understood that *Ryu*'s **p+ regions 22** are base contact regions because they: (1) correspond to the same "p+ contacts" in Ryu's other articles describing the same structure; and (2) provide low resistance ohmic contact to the p-wells 20 to short the source to the base as was well known in the art. EX1035, ¶129.

First, the **p+ regions 22** in *Ryu*'s Figure 2A correspond to the P+ regions in double-implanted MOSFETs that Ryu illustrates in prior and contemporaneous articles. *See* EX1023, Figure 1 (with *Ryu*'s Figure 2A to show the P+ regions in green); EX1024, Figure 2. EX1035, ¶130.



EX1003, FIG. 2A
(excerpted annotated)



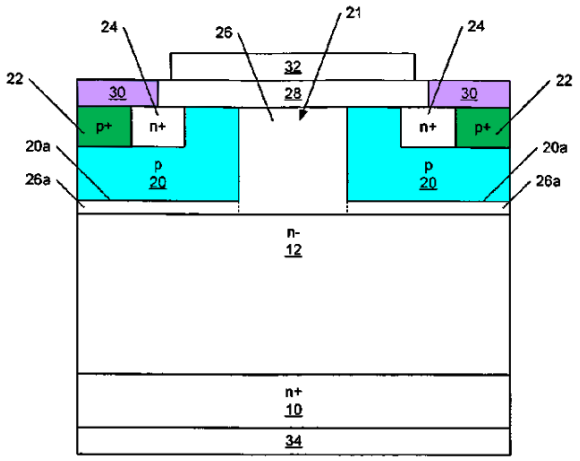
EX1023, FIG. 1
(excerpted annotated)

These P+ regions are explicitly disclosed to be "p^+ contacts to the p-wells." EX1023, 321 ("A heavy dose aluminum implantation formed ***p^+ contacts to the p-wells***,…"); EX1024, 881 (describing the same "***p^+ contacts to the p-wells***"). Like the p+ region in Ryu's articles, a POSITA would have understood *Ryu*'s **p+ regions 22** provide contacts to the p-wells 20. EX1035, ¶131.

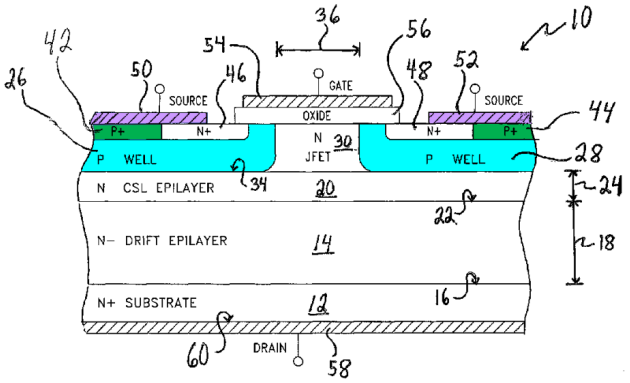
Second, a POSITA would have understood that *Ryu*'s **p+ regions 22** provide low resistance ohmic contact to the p-wells 20. *See* Section VI.D. As *Ghezzo* explains, "[a]lthough an electrical connection can be made directly to the p type base region, the p+ ***base contact region*** provides an improved connection." EX1021, 5:28–30; *see also* EX1004, 6:24–26 ("the integration of a shallow P+ region used to achieve a low resistance ohmic contact to the body"); *id.*, 16:32–34 ("maximize the ***P+ contact to the body region*** (to suppress parasitic bipolar turn-on, prevent

snapback and ruggedize the device)"); EX1006, 5:59–64 ("The base regions 11 . . . can be doped more heavily by additional implantation of aluminum for a higher latch-up strength . . . in the ***base contact region*** 12 at the source electrode 15, and thus be p+-conducting."). As exemplified by *Ghezzo*, a POSITA would have understood that *Ryu*'s p+ region provides the desired low resistance connection to the base, and is therefore a "base contact region." EX1035, ¶132.

Additionally, *Ryu*'s Figure 2A and the '633 patent's Figure 1, reproduced below, show that *Ryu*'s **p+ regions 22** and the '633 patent's "base contact regions" 42 and 44 are both p+ regions that are disposed between the **source contact** (30 for *Ryu* and 50/52 for the '633 patent) and the **P well** (20 for *Ryu* and 26/28 for the '633 patent). *Ryu*'s **p+ regions 22** have the same doping with p-type impurities as the "base contact regions" 42 and 44 of the '633 patent. EX1003, ¶¶45, 55; EX1001, 6:66–7:2. *Ryu*'s **p+ regions 22** and the '633 patent's "base contact regions" 42 and 44 both provide low resistance between the source contact and the P well. Thus, both are "base contact regions." EX1035, ¶133.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

Therefore, *Ryu* discloses element 1[h]. EX1035, ¶134.

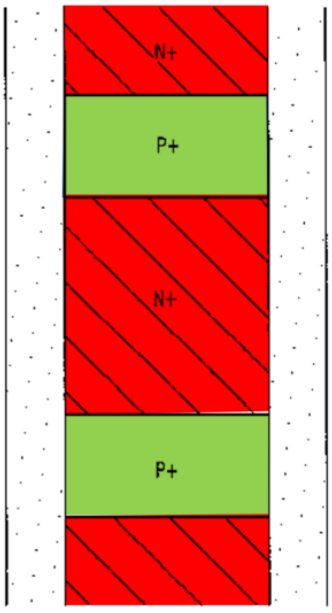
j) 1[i]: "wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions."

The combination *Ryu* and *Williams* renders element 1[i] obvious. As discussed above with respect to element 1[g], the combination of *Ryu* and *Williams* renders obvious "*a plurality of source regions*" and, with respect to element 1[h], *Ryu* discloses "*a plurality of base contact regions*." As explained below, *Ryu* also discloses **source contacts 30** formed over its left and right **n+ regions 24** (*i.e.*, "*the first source region and the second source region*"). *Ryu* does not explicitly disclose the plurality of source regions and the plurality of base contact regions forming alternating strips, which are substantially orthogonal to the **source contacts 30** formed over the left and right **n+ regions 24**. However, in view of *Williams*'s

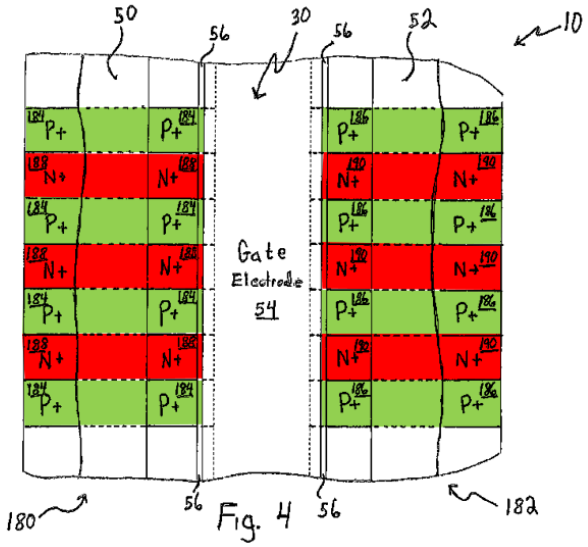
teachings, a POSITA would have found it obvious to replicate *Ryu*'s **p+ regions 22** and **n+ regions 24** to form alternating strips substantially orthogonal to the **source contacts 30**. EX1035, ¶135.

i. "the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions"

In Figure 19D (below, alongside the '633 patent's Figure 4), *Williams* discloses a "'bamboo' ladder structure (***alternating*** **N+** and **P+** regions)," like the alternating strips of **source regions 188, 190** and **base contact regions 184, 186** in the '633 patent. EX1004, 10:21–22; EX1001, Figure 4. *Williams*'s **N+ source regions** are N-typed doped regions and **P+ body contact regions** are P-type doped regions. EX1035, ¶136.



EX1004, FIG. 19D (annotated)

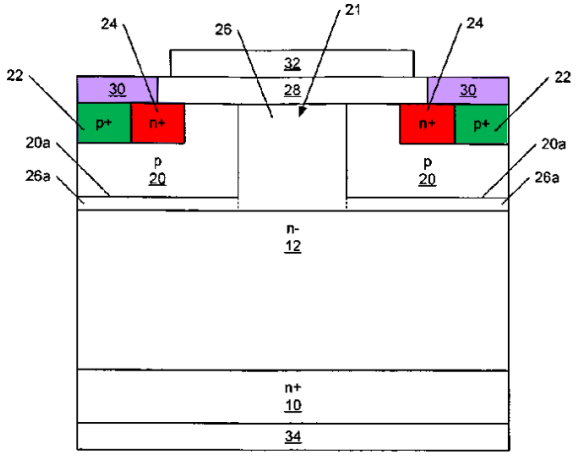


EX1001, FIG. 4 (annotated)

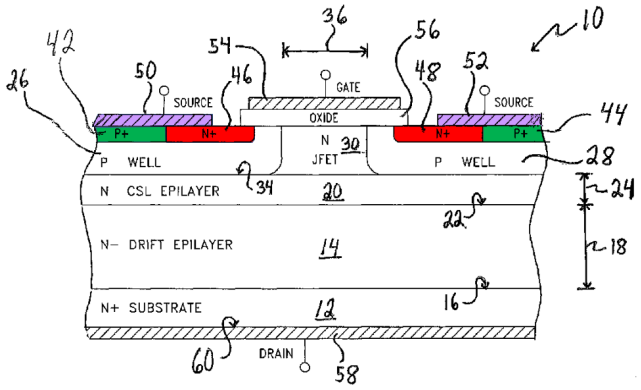
Using the same rationale as in Sections X.A.1.h.i and X.A.1.h.ii, a POSITA would have been motivated to implement *Ryu*'s MOSFET according to *Williams*'s teachings such that *Ryu*'s left and right **n+ regions 24** (*i.e.*, "*N-typed doped regions*") and **p+ regions 22** (*i.e.*, "*P-typed doped regions*") form alternating strips in a direction perpendicularly to the page. EX1035, ¶137.

ii. "source electrodes formed over the first and the second source regions"

As discussed above with respect to elements 1[d] and 1[e], *Ryu* discloses at least a left **n+ region 24** (*i.e.*, *a first source region*) and a right **n+ region 24** (*i.e.*, *a second source region*). *Ryu* also discloses that "one or more **source contacts 30**, in some embodiments are formed of nickel (Ni), titanium (Ti), platinum (Pt) or aluminum (Al), combinations thereof . . . to provide an ohmic contact to both the **p+ regions 22** and the **n+ regions 24**." EX1003, ¶47. *Ryu*'s **source contacts 30** are "source electrodes" because they are formed from a conductor and physically contact the **n+ regions 24** (*i.e.,* "source regions"). *Ryu*'s **source contacts 30** perform the same function as the '633 patent's source electrodes. *Ryu*'s Figure 2A, for example, shows that the **source contacts 30** are over the **n+ regions 24**, just like the '633 patent's **source electrodes 50 and 52** are over the **source regions 46 and 48**. *See also id.*, claims 6 and 36 ("a ***source contact on*** the first ***n-type*** silicon carbide ***region***"). EX1035, ¶138.



EX1003, FIG. 2A (annotated)

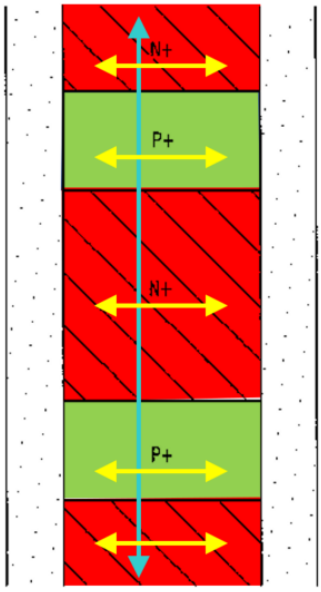


EX1001, FIG. 1 (annotated)

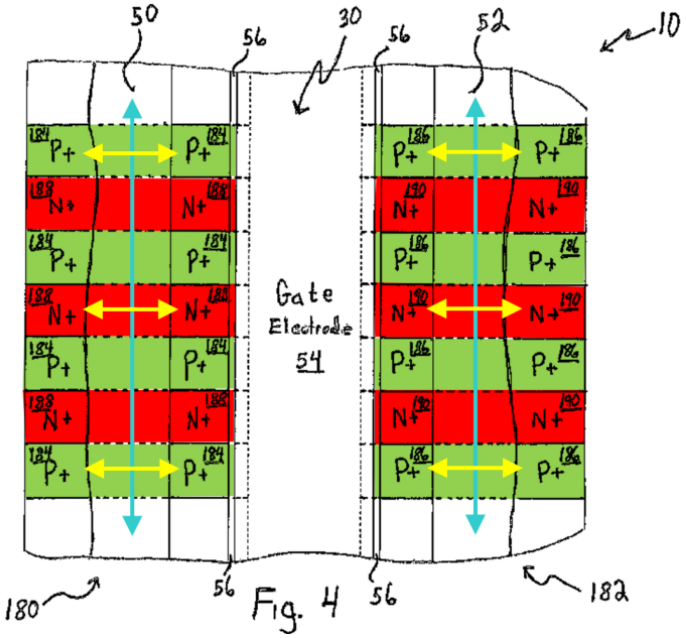
iii. "the alternating strips being substantially orthogonal to respective source electrodes"

As discussed above, a POSITA would have been motivated to implement *Ryu* in view of *Williams* such that its **n+ regions 24** and **p+ regions 22** are replicated to form alternating strips in a direction perpendicularly to the page. In such an implementation, a POSITA would also have found it obvious to form each of the **source contacts 30** to extend in the same direction to provide ohmic contact to the alternating **n+ regions 24** and **p+ regions 22**. *See* EX1003, ¶47. Moreover, as can be visualized from *Williams*'s Figure 19D plan view below (alongside the '633 patent's Figure 4 for comparison), each strip defines an axis (*i.e.*, right-left with respect to the page, shown by yellow arrows) that would be orthogonal to a source electrode that would be laid over the strips in another axis (*i.e.*, top-to-bottom with respect to the page, shown by teal arrow). Thus, in a plan view, when the **source contact 30** is extended over the alternating **n+ regions 24** and **p+ regions 22**, the

alternating **n+ regions 24** and **p+ regions 22** are substantially orthogonal to the **source contact 30**. EX1035, ¶139.



EX1004, FIG. 19D (annotated)



EX1001, FIG. 4 (annotated)

Therefore, *Ryu* in view of *Williams* renders obvious element 1[i]. EX1035, ¶140.

Accordingly, *Ryu* in view of *Williams* renders claim 1 obvious. *Id.*, ¶141.

2. Claim 2

"The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers."

Ryu in view of *Williams* renders obvious claim 1, as discussed above. *Ryu* discloses the additional limitation of claim 2. For example, *Ryu* discloses that "if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region 21** may become very high," and thus "gaps of from about 1 μm to about 10 μm are

preferred." EX1003, ¶44. Thus, *Ryu* discloses that the **JFET region 21** may have a width of less than about three micrometers because the recited width of "less than about three micrometers" is disclosed with sufficient specificity by *Ryu*'s disclosure of a JFET width "from about 1 [micrometer] to about 10 [micrometers]." EX1035, ¶142; *see also ClearValue Inc. v. Pearl River Polymers Inc.*, 668 F.3d 1340, 1345, 101 USPQ2d 1773, 1777 (Fed. Cir. 2012).

Thus, *Ryu* in view of *Williams* renders claim 2 obvious. EX1035, ¶143.

3. Claim 3

> ***"The metal-oxide semiconductor field-effect transistor of claim 2, wherein the JFET region has a width of about one micrometer."***

Ryu in view of *Williams* renders obvious claim 2, as discussed above. *Ryu* discloses the additional limitation of claim 3. For example, *Ryu* discloses that "if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region 21** may become very high," and thus "gaps of from about 1 μm to about 10 μm are preferred." EX1003, ¶44; *see also ClearValue*, 668 F.3d, 1345. Therefore, *Ryu* discloses the **JFET region 21** may have a width of about one micrometer. EX1035, ¶144.

Thus, *Ryu* in view of *Williams* renders claim 3 obvious. *Id.*, ¶145.

4. Claim 4

"The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities."

Ryu in view of *Williams* renders obvious claim 1, as discussed above. *Ryu* discloses the additional limitation of claim 4. As discussed above with respect to element 1[b], *Ryu* discloses "*the second concentration of first type impurities*" of from about 10^{14} to about 5×10^{16} cm^{-3} for the **drift layer 12**. EX1003, ¶40. And with respect to element 1[f], *Ryu* teaches "*the third concentration of first type impurities*" of from about 10^{15} to about 5×10^{17} cm^{-3} for the **JFET region 21**. *Id.*, ¶41. For example, a concentration of 5×10^{17} cm^{-3} is at least one order of magnitude greater than a concentration of 10^{14} to about 5×10^{16} cm^{-3}. EX1035, ¶146.

Thus, *Ryu* in view of *Williams* renders claim 4 obvious. *Id.*, ¶147.

5. Claim 5

"The metal-oxide semiconductor field-effect transistor of claim 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities."

Ryu in view of *Williams* renders obvious claim 1, as discussed above. *Ryu* discloses the additional limitation of claim 5. For example, *Ryu* forms **regions 26a** and the **strip** (*i.e.*, together "*the current spreading semiconductor layer*") in a region of higher carrier concentration n-type silicon carbide 26 than the **drift layer 12**.

EX1003, ¶¶41–42. Therefore, the **regions 26a** and the **strip** have the region 26's n-type (*i.e.*, "*first type impurities*") carrier concentration of "from about 10^{15} to about 5×10^{17} cm^{-3}" (*i.e.*, "*a fourth concentration*"). *Id.*, ¶41. For example, a concentration of 5×10^{17} cm^{-3} is greater than the carrier concentration of from about 10^{14} to about 5×10^{16} cm^{-3} (*i.e.*, "*the second concentration*") of the **drift layer 12**. EX1003, ¶40. EX1035, ¶148.

***Ryu* structure**	**Concentration (cm^{-3})**	**EX1003 cite**
Layer 10	About 10^{18} to about 10^{21} ("*first concentration*")	¶40
Drift layer 12	About 10^{14} to about 5×10^{16} ("*second concentration*")	¶40
JFET region 21	About 10^{15} to about 5×10^{17} ("*third concentration*")	¶41
Regions 26a and the **strip**	About 10^{15} to about 5×10^{17} ("*fourth concentration*")	¶41

Thus, *Ryu* in view of *Williams* renders claim 5 obvious. EX1035, ¶149.

6. Claim 6

"The metal-oxide semiconductor field-effect transistor of claim 5, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities."

Ryu in view of *Williams* renders obvious claim 5, as discussed above. *Ryu* discloses the additional limitation of claim 6. As discussed above with respect to claim 5, *Ryu* discloses "*the second concentration of first type impurities*" of from about 10^{14} to about 5×10^{16} cm^{-3} for the **drift layer 12**, and "*the fourth concentration of first type impurities*" of from about 10^{15} to about 5×10^{17} cm^{-3} for the **regions 26a** and the **strip**. For example, a concentration of 5×10^{17} cm^{-3} is at least one order of magnitude greater than a concentration of 10^{14} to about 5×10^{16} cm^{-3}. EX1035, ¶150.

Thus, *Ryu* in view of *Williams* renders claim 6 obvious. *Id.*, ¶151.

7. Claim 7

"The metal-oxide semiconductor field-effect transistor of claim 6, wherein the JFET region has a width of about one micrometer."

Ryu in view of *Williams* renders obvious claim 6, as discussed above. As also discussed above with respect to claim 3, *Ryu* discloses "*wherein the JFET region has a width of about one micrometer.*" EX1035, ¶152.

Thus, *Ryu* in view of *Williams* renders claim 7 obvious. *Id.*, ¶153.

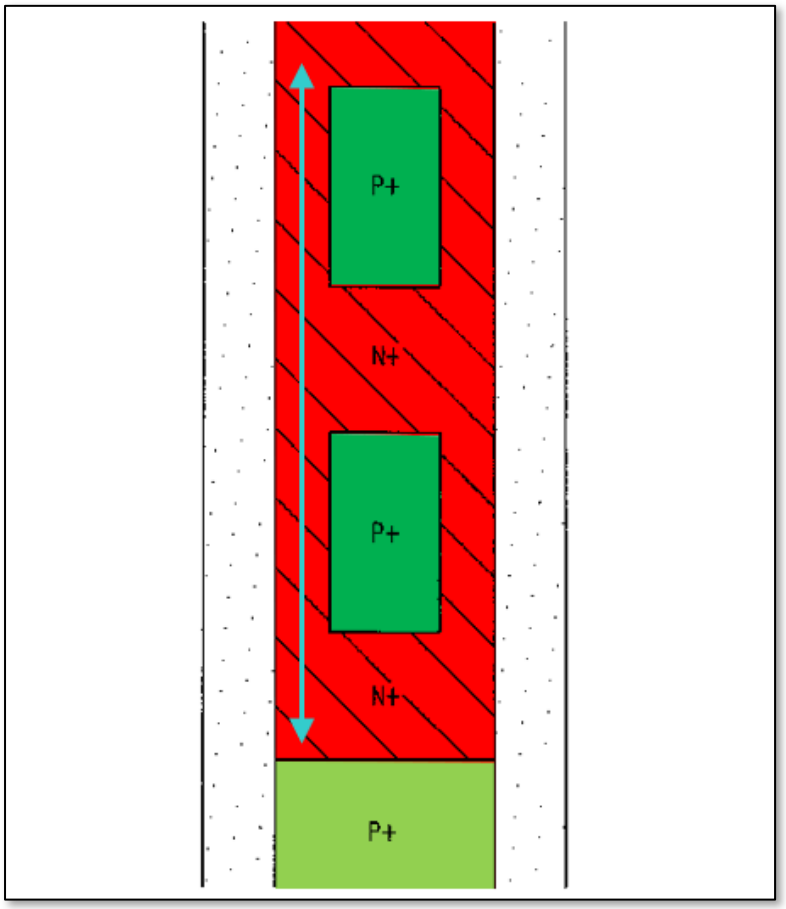
8. Claim 8

"The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions."

Ryu in view of *Williams* renders obvious claim 1, as discussed above. As also discussed above with respect to elements 1[d] and 1[e], *Ryu* discloses left and right **n+ regions 24** (*i.e.*, "*the first source region and the second source region*") and, with respect to element 1[h], *Ryu* discloses **p+ regions 22** ("*a plurality of base contact regions*"). As discussed in Sections X.A.1.h and X.A.1.j, a POSITA would have motivated to implement *Ryu*'s MOSFET according to *Williams*'s source-body ladder structure of Figure 19D such that *Ryu*'s MOSFET is formed using a linear cell structure with the **n+ regions 24** and **p+ regions 22** replicated to form alternating strips. EX1035, ¶154.

Williams also discloses, in Figure 19F (below), a source-body design that includes both "island" **P+ regions** and "strip" **P+ regions**. The "island" **P+ regions** are smaller than the surrounding **N+ source region**. While only one "strip" **P+ region** is illustrated, a POSITA would have understood that the pattern of two "island" **P+ regions** and one "strip" **P+ region** would repeat along an axis (*i.e.*, up-down with respect to the page, shown by teal arrow). *Williams* notes that the design of Figure 19F provides "better N+ contact resistance." EX1004, 17:15–18.

Therefore, using the same rationale as in Sections X.A.1.h.i and X.A.1.h.ii, if the design goal were to prioritize reduced on-resistance over device ruggedness, a POSITA would have been motivated by *Williams*'s layout of Figure 19F to further modify the shape and location of *Ryu*'s **p+ regions 22** such that, in addition to forming alternating strips with the **n+ regions 24**, the **p+ regions 22** would also form a plurality of islands that are smaller than the **n+ regions 24**. Such a configuration would increase the area of *Ryu*'s **n+ regions 24**, thereby reducing the source-contact resistance and the overall on-resistance of *Ryu*'s MOSFET. EX1035, ¶155.



EX1004, FIG. 19F (annotated)

Thus, *Ryu* in view of *Williams* renders claim 8 obvious. EX1035, ¶156.

9. Claim 12

a) 12[preamble]: "A double-implanted metal-oxide semiconductor field-effect transistor comprising:"

Regardless of whether the preamble is limiting, *Ryu* discloses it. As discussed above with respect to element 1[preamble], *Ryu* discloses a "*metal-oxide semiconductor field-effect transistor*." Moreover, *Ryu*'s MOSFET is doubly implanted. *Ryu* explains that, during the fabrication process of its MOSFET, using a mask 100, "impurities are implanted into the n-type epitaxial layer 26 to provide the p-wells 20," and in the next step of the process, "n-type impurities are implanted utilizing the mask 104 to provide the n+ regions 24." EX1003, ¶¶53–54, Figures 4B and 4C; *cf.* EX1021, 1:56–63 ("***double ion implantation sequence*** . . . by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) ***to form the base and source regions***, respectively."); EX1020, 960 ("DMOS structure is formed in SiC using a ***double ion implantation with two separate implantation masks***."); EX1022, 659. *Ryu*'s doubly implanted p-wells 20 and n+ regions 24 configuration is also the same as in the "Vertical ***Doubly Implanted MOSFET*** (DIMOSFET)" that *Ryu* illustrates in Figure 1. EX1003, ¶¶6, 27, Figure 1. EX1035, ¶157.

Therefore, *Ryu* discloses the preamble. *Id.*, ¶158.

b) 12[a]: "a semiconductor substrate;"

Ryu discloses element 12[a] for the same reasons discussed above for element 1[a]. EX1035, ¶159.

c) 12[b]: "a drift semiconductor layer formed on a front side of the semiconductor substrate;"

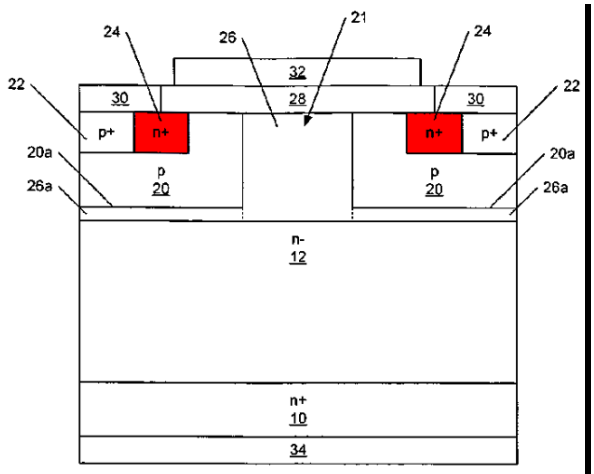
Ryu discloses element 12[b] for the same reasons discussed above for element 1[b]. EX1035, ¶160.

d) 12[c]: "a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;"

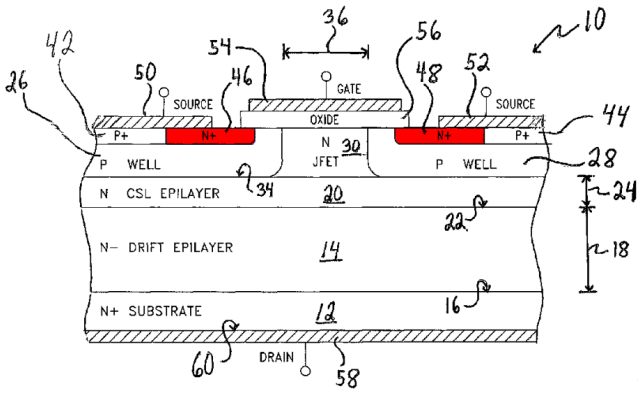
Ryu discloses element 12[c] for the same reasons discussed above for element 1[c]. EX1035, ¶161.

e) 12[d]: "a plurality of first and second source regions;"

The combination *Ryu* and *Williams* renders element 12[d] obvious. As discussed above with respect to elements 1[d] and 1[e], *Ryu* discloses at least a left **n+ region 24** (*i.e.*, *a first source region*) and a right **n+ region 24** (*i.e.*, *a second source region*), as *Ryu* illustrates in Figure 2A, reproduced below alongside the '633 patent's Figure 1. EX1035, ¶162.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

Ryu does not explicitly disclose a plurality of first and second source regions. However, using the same rationale as in Sections X.A.1.h and X.A.1.j, a POSITA would have been motivated to implement *Ryu*'s MOSFET according to *Williams*'s teachings such that *Ryu*'s MOSFET is formed using a linear cell structure having, from a plan or top view, the left **n+ region 24** and a right **n+ region 24** replicated and spaced apart as strips, alternatingly with strips of **p+ regions 22**, to form a plurality of first and second source regions. EX1035, ¶163.

f) 12[e]: "a plurality of base contact regions; and"

Ryu discloses element 12[c] for the same reasons discussed above for element 1[h]. EX1035, ¶164.

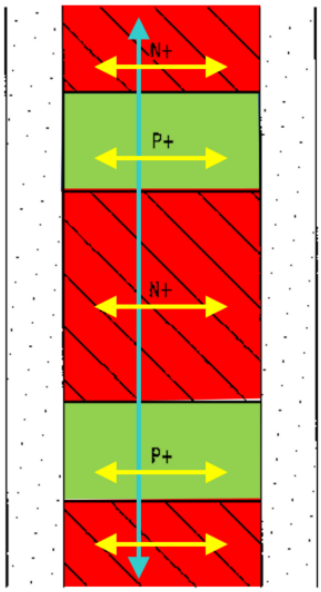
g) 12[f]: "a JFET region defined between the plurality of first source regions and the plurality of second source regions, the JFET region being formed on a front side of the current spreading semiconductor layer,"

The combination *Ryu* and *Williams* renders element 12[f] obvious. As discussed above with respect to element 12[d], a POSITA would have been motivated to implement *Ryu*'s MOSFET according to *Williams*'s teachings such that *Ryu*'s MOSFET is formed using a linear cell structure having, from a plan or top view, the left **n+ region 24** and the right **n+ region 24** replicated and spaced apart to form a plurality of first and second source regions. Because *Ryu*'s **JFET region 21** is between the left **n+ region 24** and the right **n+ region 24** (*see* Section X.A.1.g.iii), the **JFET region 21** would also be defined between the plurality of first and second source regions. *Ryu*'s **JFET region 21** is also formed on the front side of **regions 26a** and the **strip** (*i.e.*, "*the current spreading semiconductor layer*"). *See* Section X.A.1.g.ii. EX1035, ¶165.

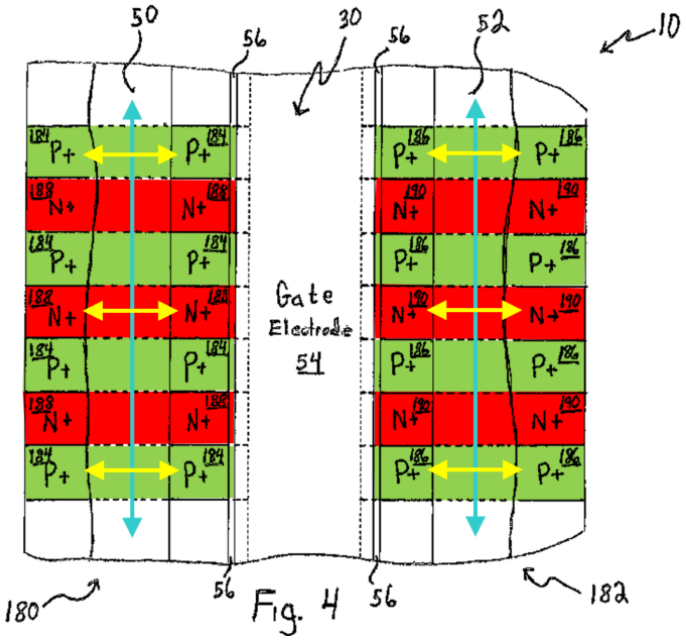
h) 12[g]: "wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions."

The combination *Ryu* and *Williams* renders element 12[g] obvious. As discussed above with respect to element 12[d], the combination of *Ryu* and *Williams* renders obvious "*a plurality of first and second source regions*" and, with respect to

element 12[e], *Ryu* discloses "*a plurality of base contact regions*." *Ryu* also discloses a **source contact 30** formed over each of its left **n+ region 24** (*i.e.*, *the first source region*) and right **n+ region 24** (*i.e.*, *a second source region*). *See* Section X.A.1.j.ii. Using the same rationale as in Sections X.A.1.h and X.A.1.j, a POSITA would have been motivated to implement *Ryu*'s MOSFET according to *Williams*'s teachings such that *Ryu*'s MOSFET is formed using a linear cell structure having, from a plan or top view, the plurality of first and second source regions and the plurality of base contact regions form alternating strips, with each of the **source contacts 30** extending and overlying over a set of alternating strips. Moreover, as can be visualized from *Williams*'s Figure 19D plan view below (alongside the '633 patent's Figure 4 for comparison), each strip defines a longitudinal axis (*i.e.*, right-left with respect to the page) that would be orthogonal to a source electrode that would be laid over the strips in another longitudinal axis (*i.e.*, top-to-bottom with respect to the page). Thus, in a plan view, each of the alternating strip defines a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by the **source contact 30**. EX1035, ¶166.



EX1004, FIG. 19D (annotated)



EX1001, FIG. 4 (annotated)

Therefore, *Ryu* in view of *Williams* renders obvious element 12[g]. EX1035, ¶167.

Accordingly, *Ryu* in view of *Williams* renders obvious claim 12. *Id.*, ¶168.

10. Claim 13

> ***"The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities."***

Ryu in view of *Williams* renders obvious claim 12, as discussed above. *Ryu* discloses the additional limitation of claim 13. As discussed above with respect to claim 5, *Ryu*'s **regions 26a** and the **strip** (*i.e.*, "*the current spreading semiconductor layer*") has an n-type (*i.e.*, "*first type impurities*") carrier concentration of from about

10^{15} to about $5\times10^{17}\,cm^{-3}$ (*i.e.*, "*a first concentration*"). EX1003, ¶¶41–42. As also discussed above, with respect to element 1[b], *Ryu* discloses that the n− (*i.e.*, "*first type impurities*") **drift layer 12** has a carrier concentration of from about 10^{14} to about $5\times10^{16}\,cm^{-3}$ (*i.e.*, "*a second concentration*"). EX1003, ¶40. For example, a concentration of $5\times10^{17}\,cm^{-3}$ is greater than a concentration of about 10^{14} to about $5\times10^{16}\,cm^{-3}$. EX1035, ¶169.

Thus, *Ryu* in view of *Williams* renders claim 13 obvious. *Id.*, ¶170.

11. Claim 14

> ***"The double-implanted metal-oxide semiconductor field-effect transistor of claim 13, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities."***

Ryu in view of *Williams* renders obvious claim 13, as discussed above. *Ryu* discloses the additional limitation of claim 14. For example, a concentration of $5\times10^{17}\,cm^{-3}$ is at least one order of magnitude greater than a concentration of about 10^{14} to about $5\times10^{16}\,cm^{-3}$. EX1035, ¶171.

Thus, *Ryu* in view of *Williams* renders claim 14 obvious. *Id.*, ¶172.

12. Claim 15

"The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about three micrometers or less."

Ryu in view of *Williams* renders obvious claim 12, as discussed above. As also discussed above with respect to claim 2, *Ryu* discloses "*wherein the JFET region has a width of about three micrometers or less.*" EX1035, ¶173.

Thus, *Ryu* in view of *Williams* renders claim 15 obvious. *Id.*, ¶174.

XI. CO-PENDING DISTRICT COURT LITIGATION IN TEXAS SHOULD NOT PRECLUDE INSTITUTION

Although there is concurrent district court litigation involving the '633 patent, the weight of the factors described in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) favors institution of this Petition.

A. The potential for a stay of the district court case urges against denial (factor 1)

After at least any institution of review based on this Petition, ST intends to seek a stay of the co-pending district court proceedings. Therefore, factor 1 is neutral because any decision by the district court to stay the case would issue after institution and be based on "a variety of circumstances and facts beyond [the Board's] control and to which the Board is not privy." *See Sand Revolution II, LLC v. Cont'l*

Intermodal Grp. Trucking, LLC, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative).

B. Uncertainty over the trial date in the Texas case favors institution (factor 2)

The district court recently entered a Scheduling Order identifying April 24, 2023 as the target trial date. EX1026, 5. Based on the expected 18-month IPR schedule, a final written decision (FWD) in this proceeding would likely issue by September 2023. However, this factor favors institution, or is neutral, because the district court's trial date is subject to considerable uncertainty. *Sand Revolution*, IPR2019-01393, Paper 24 at 9-10 (uncertainty of trial date weighed in favor of institution) (informative); *Micron Tech., Inc. v. Godo Kaisha IP Bridge 1*, IPR2020-01008, Paper 10 at 14 (PTAB Dec. 7, 2020).

Despite the district court's aspirational target date, trial is unlikely to begin on April 24, 2023 and may be postponed until after the Board issues a FWD in this proceeding. *E.g.,* EX1034 (the court's crowded docket, including over 834 pending patent cases); EX1028, 3 ("In the WDTX, 70% of trial dates initially relied upon by the PTAB to deny petitions have slid.").

In contrast to the potential delays to the district court's schedule, the Board's schedule is unlikely to shift. 35 U.S.C. § 316(a)(11) (one-year statutory deadline for FWD); *Sand Revolution*, IPR2019-01393, Paper 24 at 9. Given the circumstances,

the Board may well issue a FWD before the beginning of any trial in the district court.

Factor 2 also favors institution because ST diligently filed this Petition ***nearly four months*** before its statutory deadline for doing so. *See, e.g.*, *Apple Inc. v.Seven Networks, LLC*, IPR2020-00156, Paper 10 at 9 & n.8 (PTAB June 15, 2020) (considering the filing date relative to potential filing dates helps to analyze factor 2 on a sliding scale based on relative trial dates).

C. Investment in the parallel district court proceeding is minimal and ST was diligent in filing this Petition (factor 3)

The co-pending district court case is still in an early phase. The court has not addressed the merits of the case. All significant stages of litigation—including discovery, claim construction, summary judgment, and trial—remain in the future. The target trial date is 13 months away and will likely be delayed. After receiving at least any institution decision, ST intends to move for a stay in the district court to further minimize investment by the court and the parties.

D. The Petition raises unique issues, which favors institution (factor 4)

ST expects its invalidity positions in the district court case will diverge from the ground of unpatentability described in this Petition. At the time of filing this Petition, the claims challenged herein have not been asserted against ST and are not being litigated in the district court. In any event, ST reserves the right to enter a

stipulation relating to the district court case that would prevent and/or reduce overlap with the requested IPR, should the Board deem one necessary. *See Sand Revolution*, IPR2019-01393, Paper 24 at 12.

E. The parties overlap (factor 5)

The district court case and the IPR proceeding involve the same parties.

F. The merits of ST's challenge support institution (factor 6)

As described above, *Ryu* and *Williams* disclose and render obvious the allegedly inventive features of the '633 patent, including the configuration recited by claims 1–8 and 12–15. The merits of the prior art and their close correspondence to the challenged claims favors institution. *Fintiv*, IPR2020-00019, Paper 11 at 14-15.

XII. CONCLUSION

Petitioner requests institution of an IPR of the ’633 patent and cancellation of claims 1–8 and 12–15.

Respectfully Submitted,

Dated: March 25, 2022

/Scott Bertulli/
Scott Bertulli, Lead Counsel
Registration No. 75,886

TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 7,498,633
1002	[Reserved]
1003	U.S. Patent Application Publication No. 2004/0119076 ("*Ryu*")
1004	U.S. Patent No. 6,413,822 ("*Williams*")
1005	U.S. Patent No. 5,233,215 ("*Baliga*")
1006	U.S. Patent No. 6,316,791 ("*Schörner*")
1007	U.S. Patent Application No. 2006/0267092 ("*Jun*")
1008	'633 Patent File History, 4/4/2007 Non-Final Rejection
1009	'633 Patent File History, 8/6/2007 Response to Office Action
1010	'633 Patent File History, 10/12/2007 Final Rejection
1011	'633 Patent File History, 3/12/2008 Response to Office Action
1012	'633 Patent File History, 6/25/2008 Non-Final Rejection
1013	'633 Patent File History, 8/22/2008 Response to Office Action
1014	'633 Patent File History, 12/17/2008 Notice of Allowance
1015	U.S. Patent No. 5,317,184 ("*Rexer*")
1016	[Reserved]
1017	A. G. Jost et al., "Implementation of a VLSI Layout Tool on Personal Computers," ACM, 1990

Exhibit	Description
1018	E. S. Kuh et al., "Recent Advances in VLSI Layout," Proceedings of the IEEE, vol 78, no. 2, February 1990
1019	"Power MOSFETs – Theory and Applications," Duncan A. Grant and John Gowar, 1989 ("*Grant*") (relevant sections)
1020	J. A. Cooper, Jr. et al., "SiC Power-Switching Devices—The Second Electronics Revolution?," Proceedings of the IEEE, vol. 90, no. 6, June 2002
1021	U.S. Patent No. 5,510,281 ("*Ghezzo*")
1022	J. A. Cooper, Jr. et al., "Status and Prospects for SiC Power MOSFETs," IEEE Transactions on Electron Devices, vol. 49, no. 4, April 2002
1023	S-H Ryu et al., "10 A, 2.4 kV Power DiMOSFETs in 4H-SiC," IEEE Electron Device Letters, vol. 23, no. 6, June 2002
1024	S-H Ryu et al., "2 kV 4H-SiC DMOSFETs for Low Loss, High Frequency Switching Applications," International Journal of High Speed Electronics and Systems, vol. 14, no. 3, 2004
1025	[Reserved]
1026	Scheduling Order, *The Trustees of Purdue University v. STMicroelectronics, Inc. et al.*, No. 6:21-cv-00727 (W.D. Tex.), Dkt. 45 (November 22, 2021)
1027	[Reserved]
1028	Article entitled "District Court Trial Dates Tend to Slip After PTAB Discretionary Denials" (July 24, 2020)
1029	U.S. Patent Application Publication No. 2005/0023607

Exhibit	Description
1030	U.S. Patent No. 6,570,185 ("*Tan*1")
1031	J. Tan et al., "High-Voltage Accumulation-Layer UMOSFET's in 4H-SiC," IEEE Electron Device Letters, vol. 19, no. 12, December 1998 ("*Tan*2")
1032	"Modern Power Devices," B. Jayant Baliga, 1987 (relevant sections)
1033	S-H Ryu et al., "Design and Process Issues for Silicon Carbide Power DiMOSFETS," Mat. Res. Soc. Symp., vol. 640, 2001
1034	Statistics from Docket Navigator showing active patent cases before Judge Alan Albright of the U.S. District Court for the Western Digital of Texas (as of March 25, 2022)
1035	Declaration of Dr. Vivek Subramanian

CERTIFICATE UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,936, which is less than the 14,000 words allowed under 37 CFR § 42.24(a)(1)(i).

Respectfully submitted,

DATED: March 25, 2022

/Scott Bertulli/
Scott Bertulli
Reg. No. 75,886

CERTIFICATE OF SERVICE

I hereby certify that on March 25, 2022, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,498,633 under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibit List
- Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 7,498,633 (EX1001–EX1035)
- Power of Attorney
- Fee Authorization
- Word Count Certification Under 37 CFR § 42.24(d)

to be served via Express Mail on the following correspondent of record as listed on PAIR:

Barnes & Thornburg LLP
11 S. Meridian Street
Indianapolis IN 46204

DATED: March 25, 2022

/Scott Bertulli/
Scott Bertulli
Reg. No. 75,886